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# MS-7B28

ATX:230mm\*185mm

## Intel -CoffeeLake-S plamform

### CPU:

LGA1151

CPU POWER PAK \*4Phase

GT POWER PAK \*2 Phase

### Onboard Chip:

SIO: NUVOTON 5567

HD Audio Codec: ALC887

LAN: INTEL I219V

Flash ROM: SPI 64 MB

CUT VBAT:SLG4B41231

### Main Memory:

DDR4 \* 2 (Dual Channel)

### ACPI:

5VDAUL:uP7501

5VDIMM:uP7501

3VSB:GS7133+N MOS

1P8\_VSB:GS7166

3VDSW:L11831

VCCSTPLL:GS7133

### Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1 ) Slot \* 2

### System Chipset:

H310

### PWM:

VCORE - RT3607	138A
VGT- RT3607	45A
DDR - RT8231	11.525A
DDR VPP25- MP2143	1.12A
PCH(1.05V) - RT8125E	10.743A
VCCSA - RT8125E	11.1A
VCCIO - SY8288	6.4A

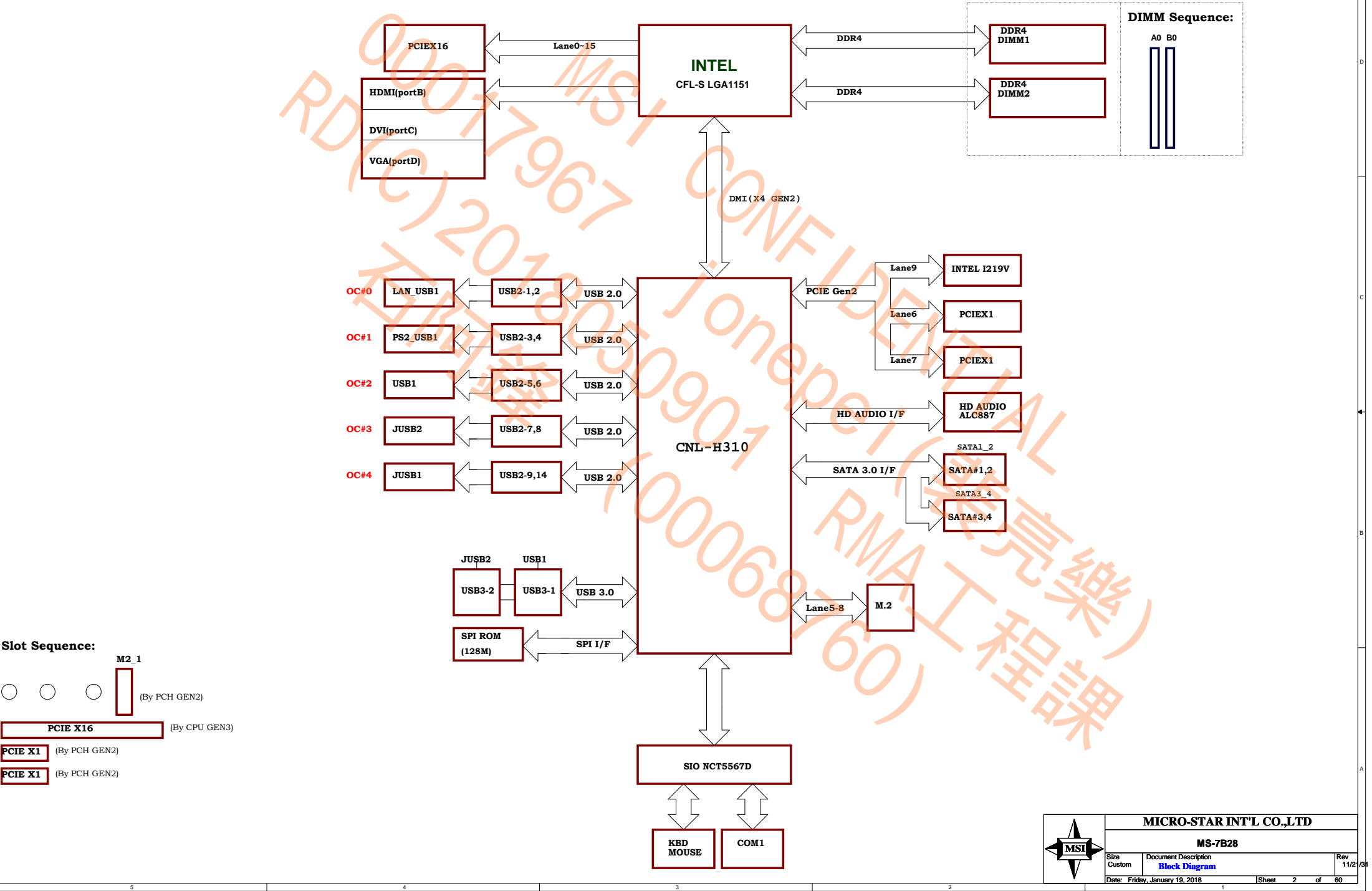


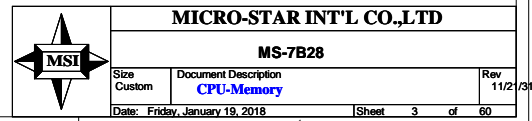
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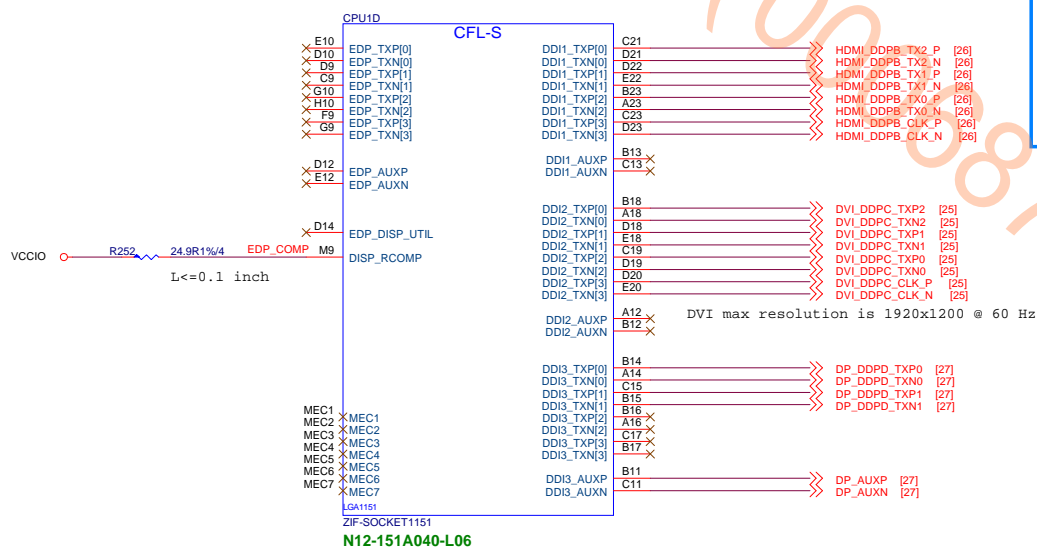
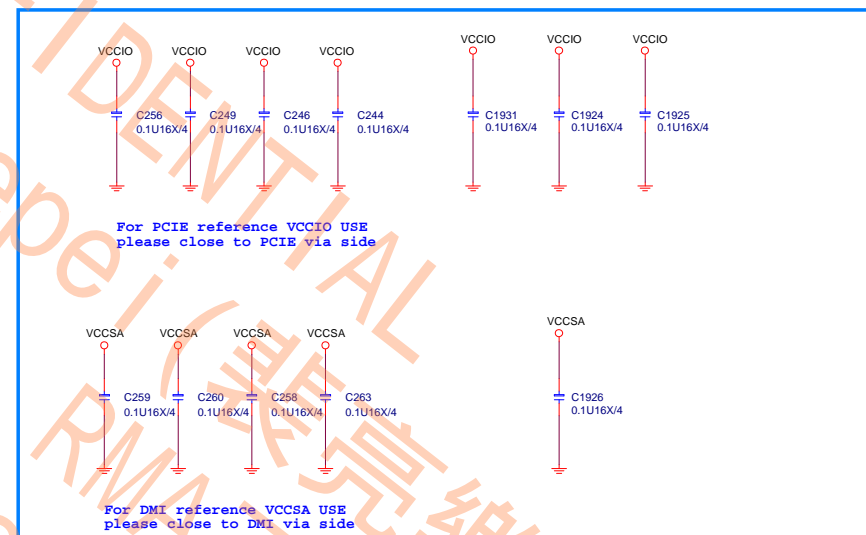
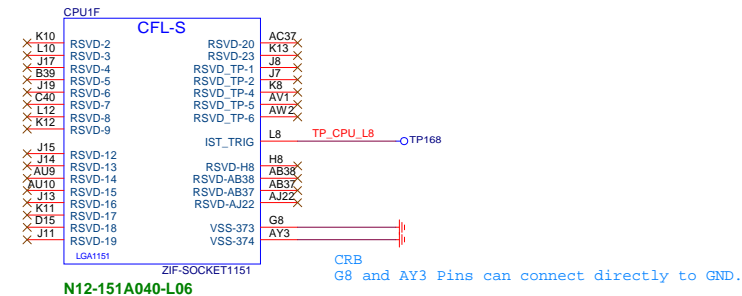
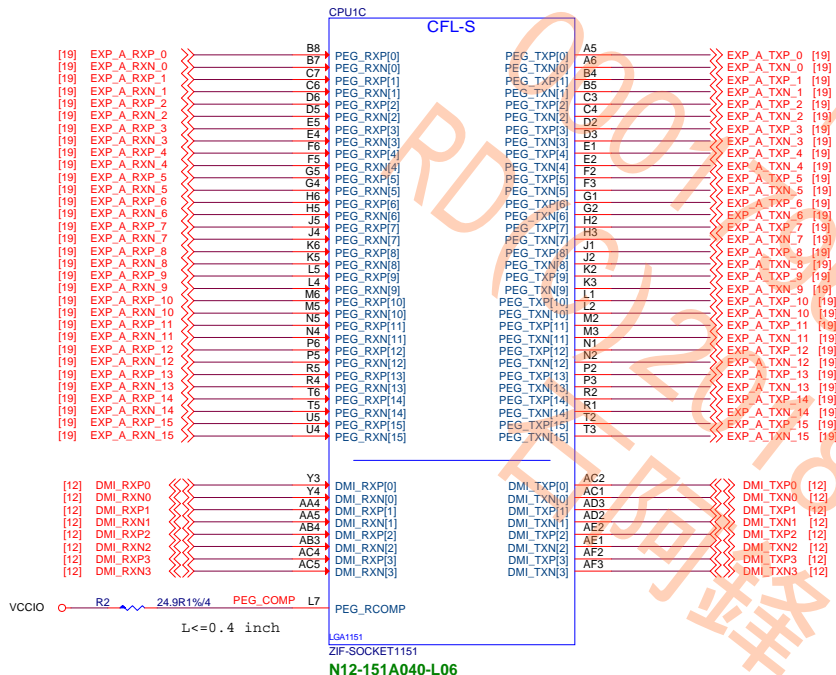
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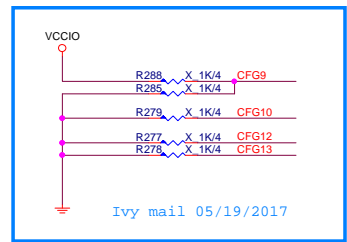
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Block Diagram

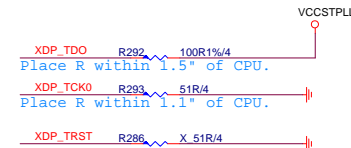
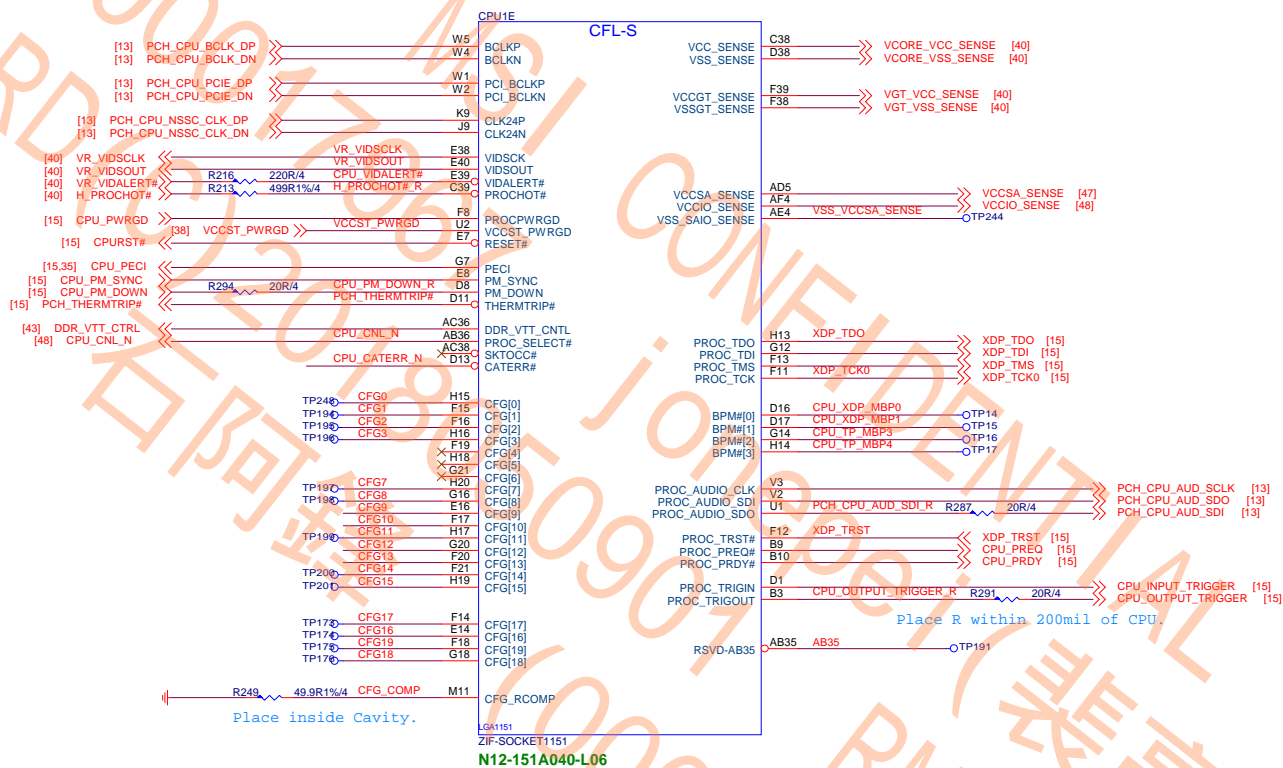
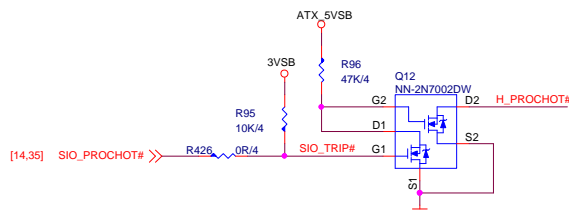
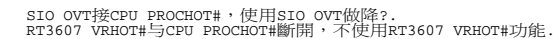








	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU P/L Lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PGD/CFGSEL[0]
6	DISABLE	ENABLE	PGD/CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEVR. TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		



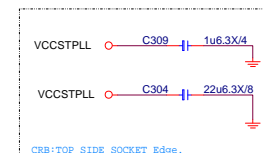
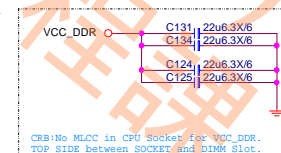
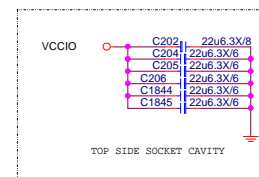
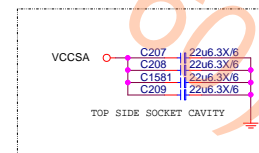
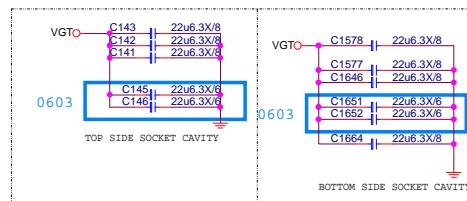
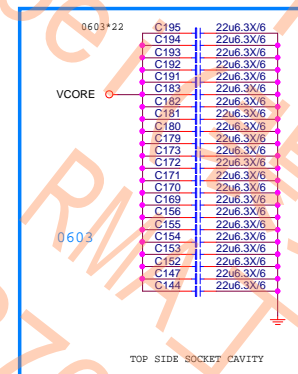
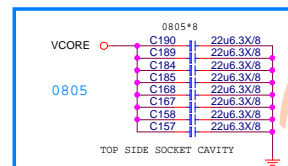
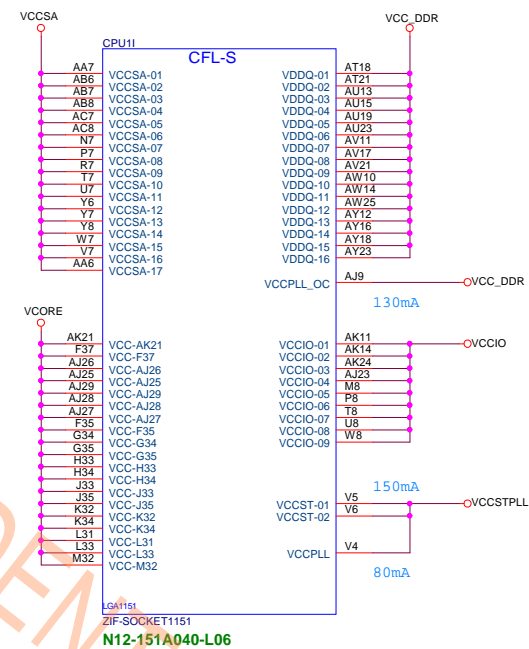
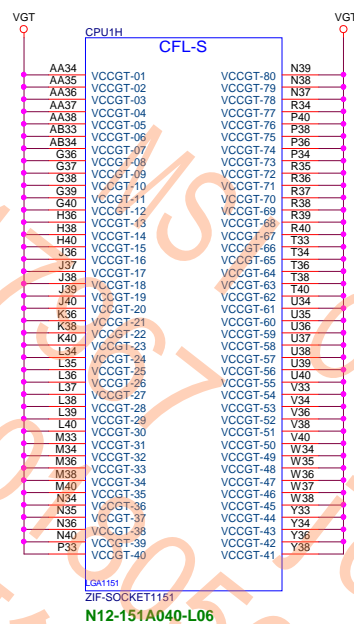
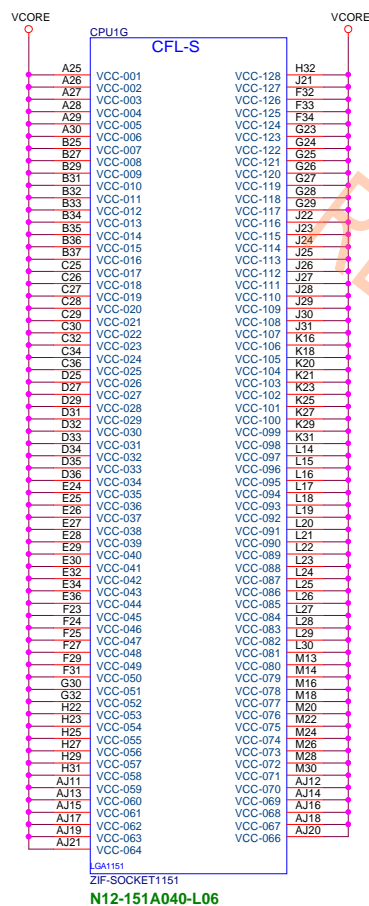
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Size Custom	Document Description <b>CPU-Control/MISC/CFG/Audio</b>	Rev 11/2/3
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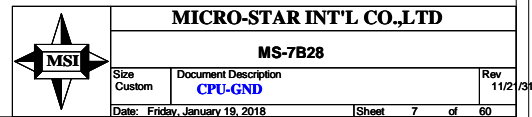


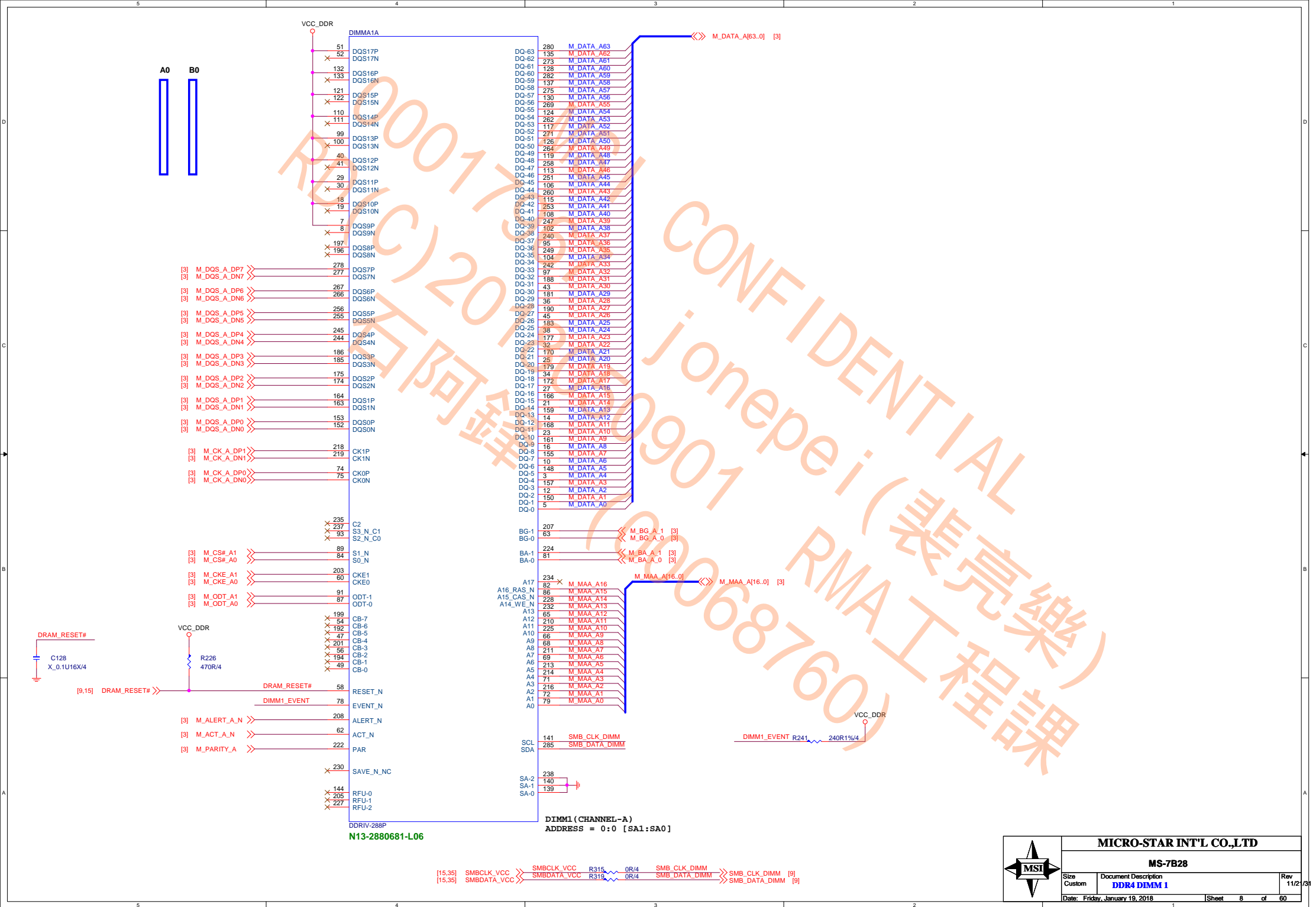


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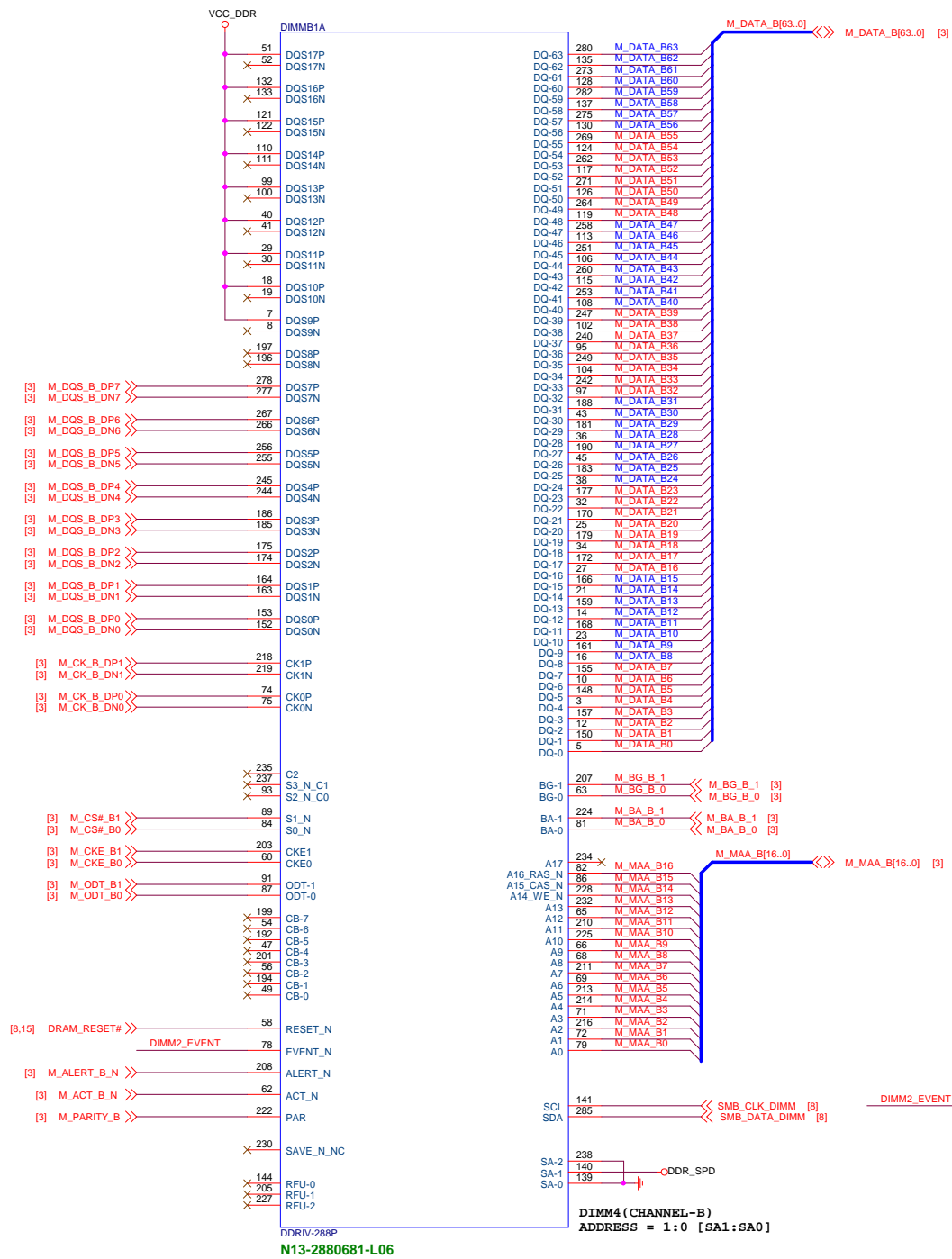
MS-7B28


Size Custom	Document Description <b>CPU-Power</b>	Rev 11/2/3
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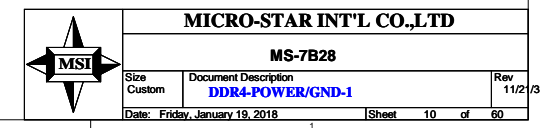
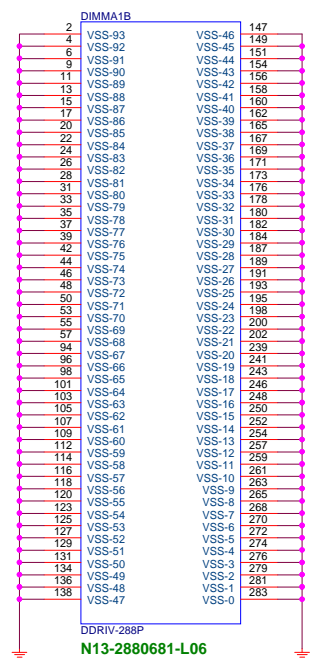
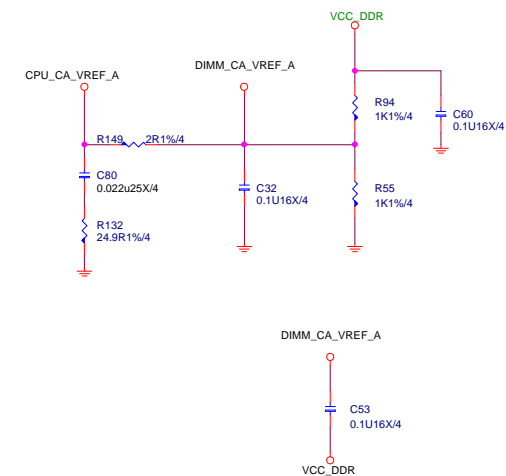
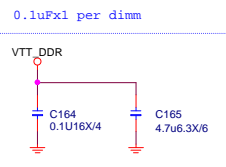
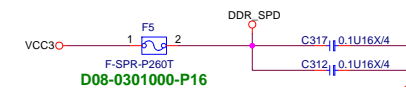


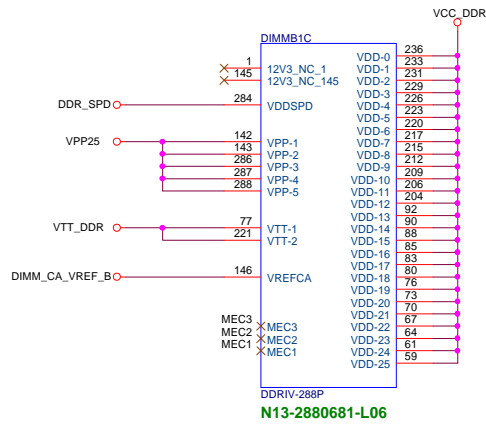




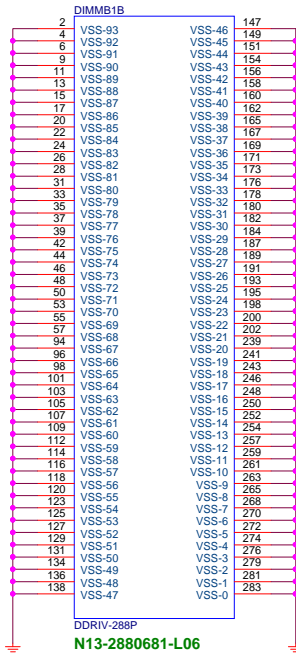
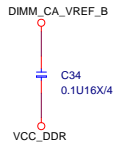
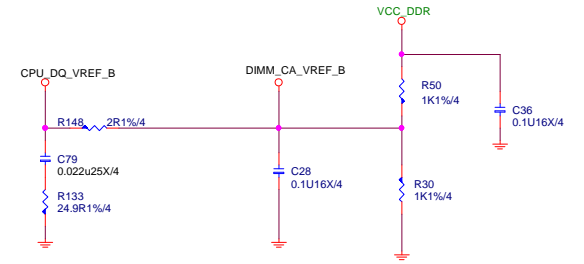
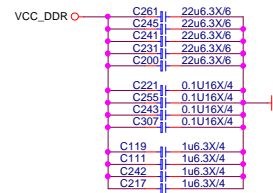
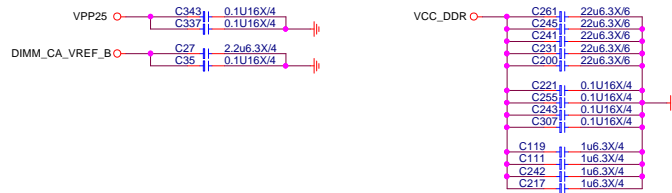
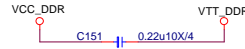


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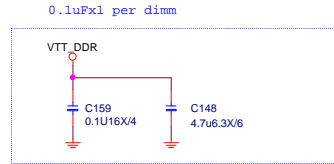


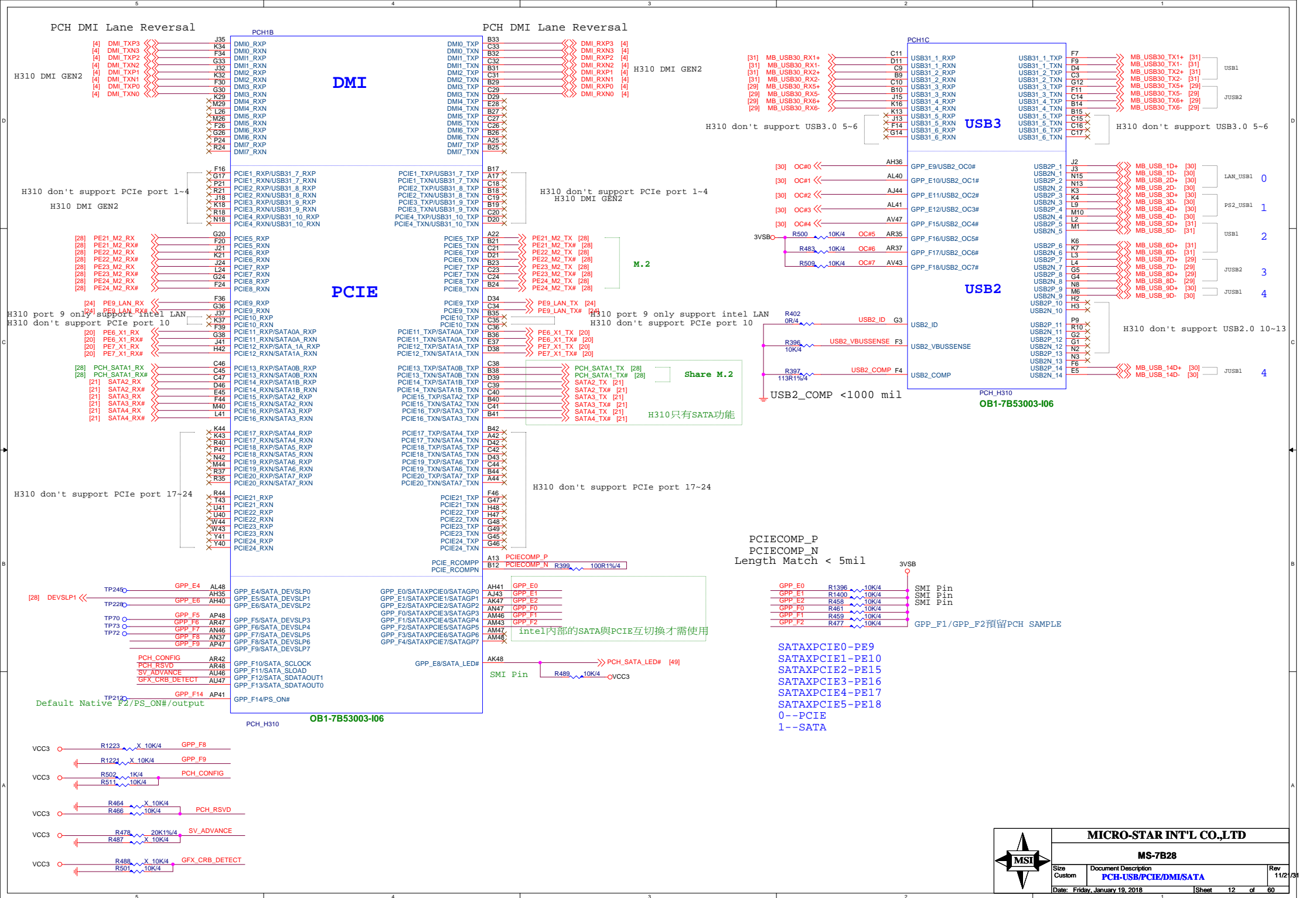


DDRIV-288P  
**N13-2880681-L06**

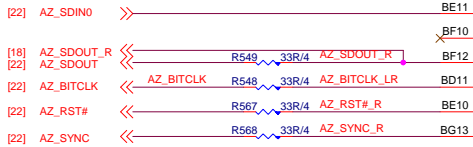
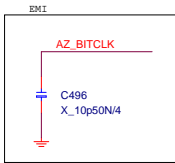
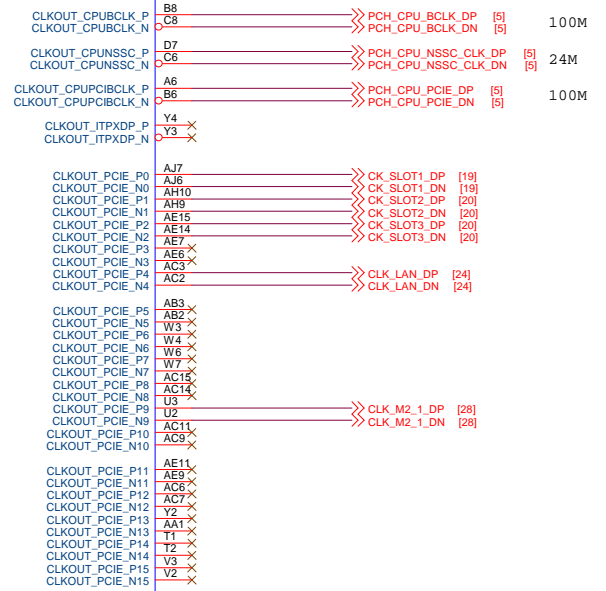
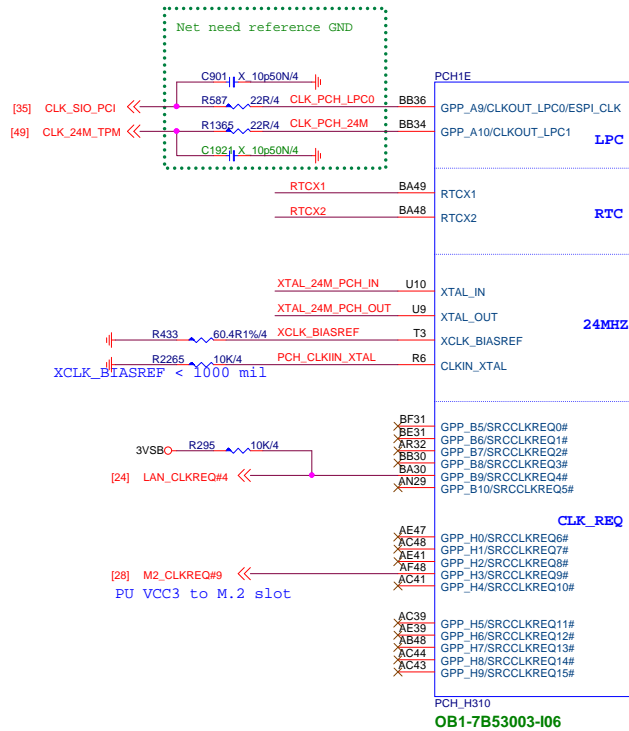
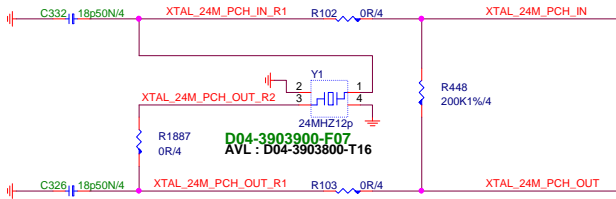
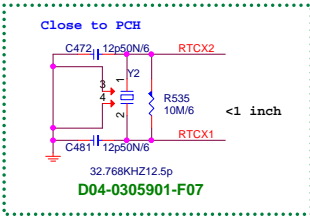


DDRIV-288P  
**N13-2880681-L06**



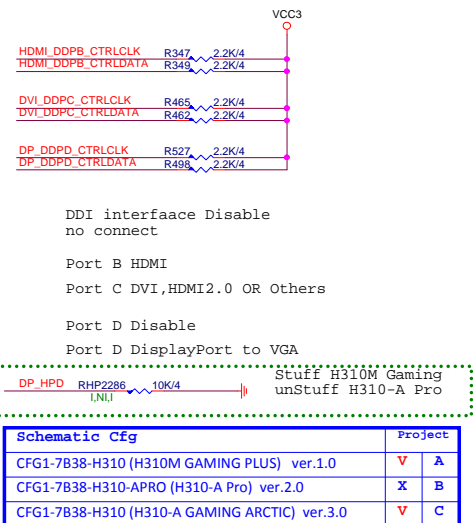
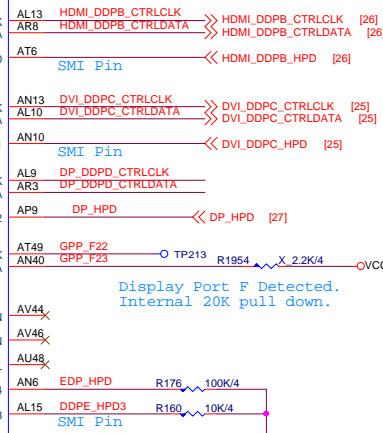
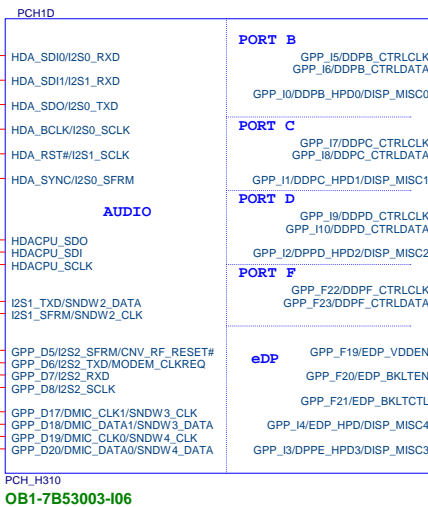


## RTC Block



Default Native F3/CNV\_RF\_R\_ESET#.

Default Native F3/MODEM\_CLKREQ.

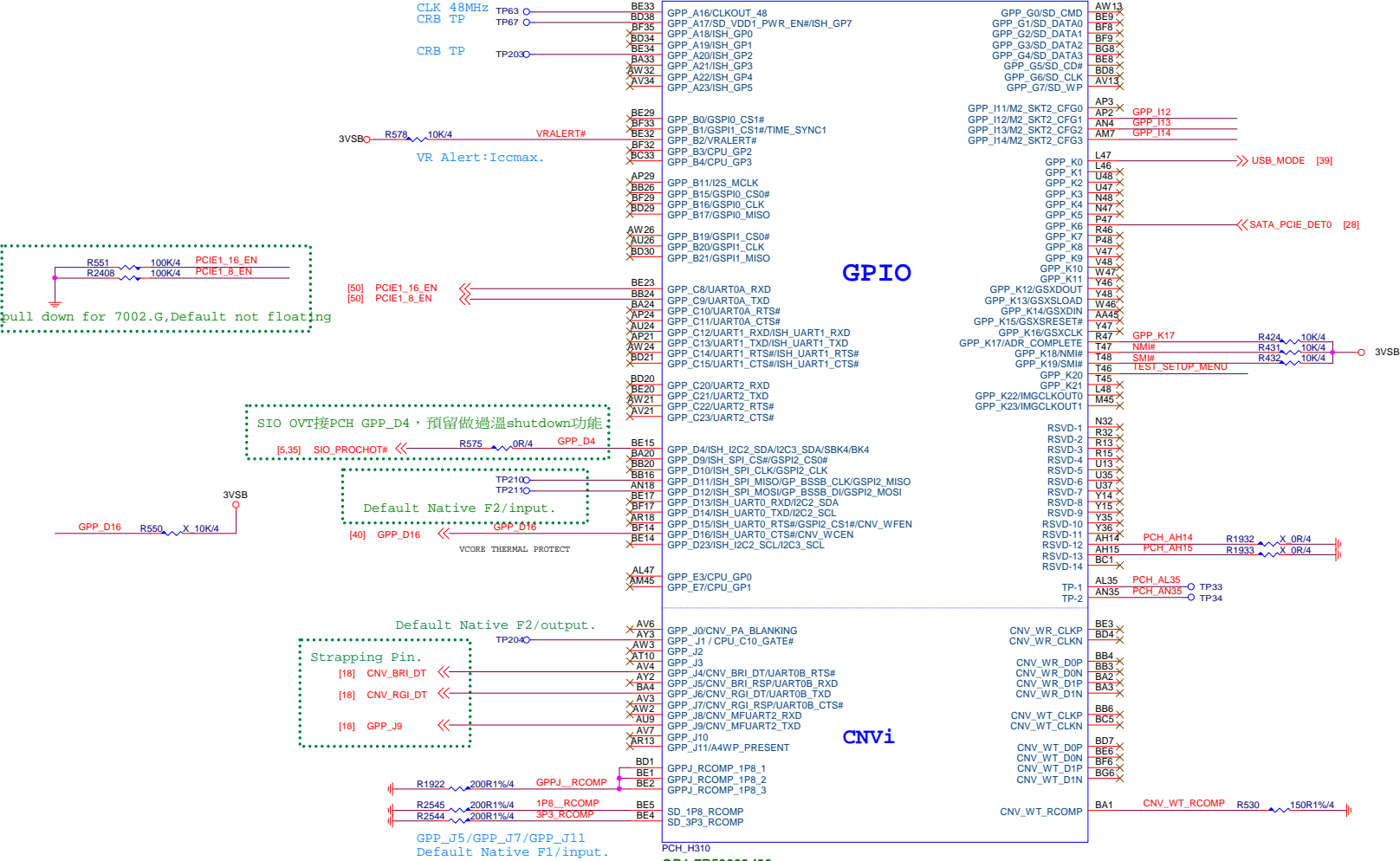


Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V C

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Custom	PCH-Audio/Display/Clock	11/2
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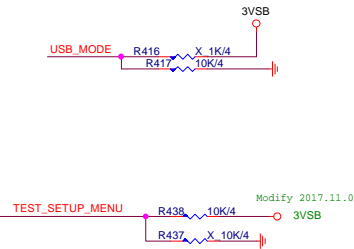


GPIO (SMI/NMI):  
GPP\_B14, GPP\_B20, GPP\_B23  
GPP\_C[23:22]  
GPP\_D[4:0]  
GPP\_E[8:0]  
GPP\_I[3:0]  
GPP\_G[7:0] (Support SMI# only)



	GPP_I12	GPP_I13	GPP_I14
H310_GPLUS	0	0	0
H310_APRO	0	0	1
H310_GARCTIC	0	1	0

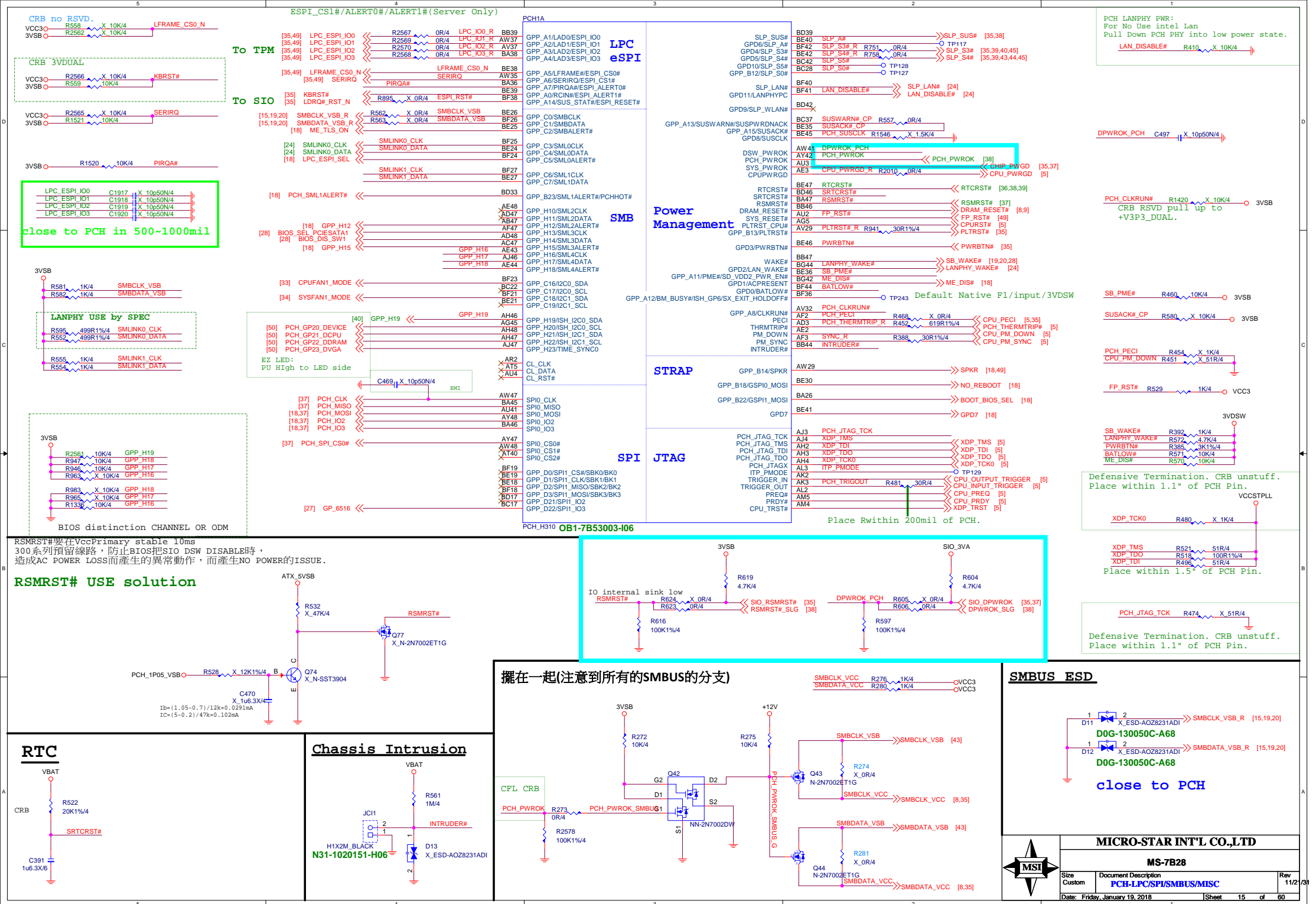
For BIOS BOM USE

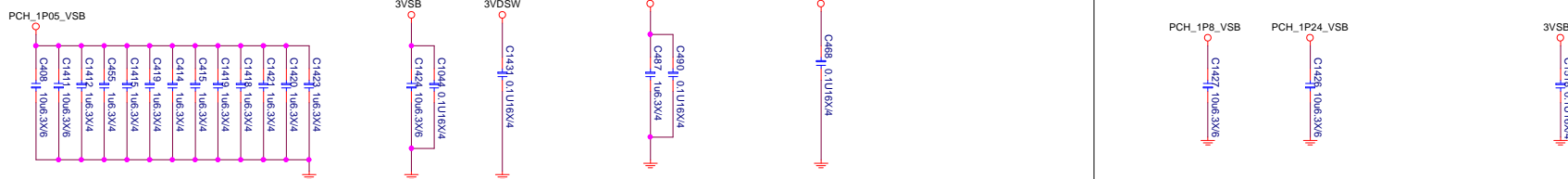
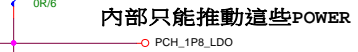
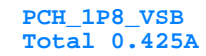
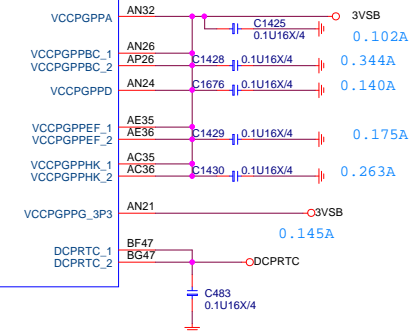
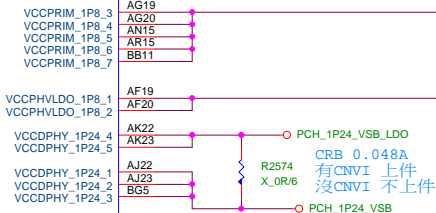
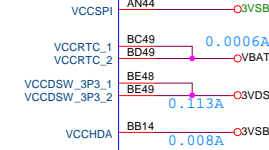
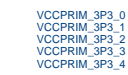
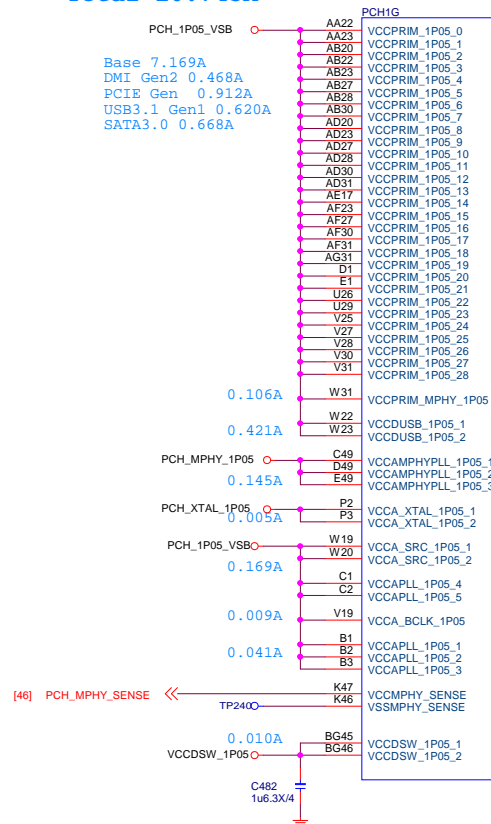
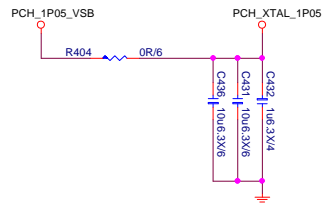
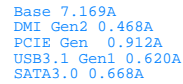


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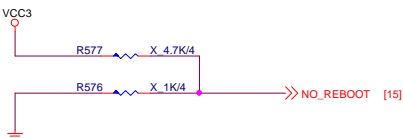


TOP Swap



Internal pull-down 20K is disabled after PLTRST#

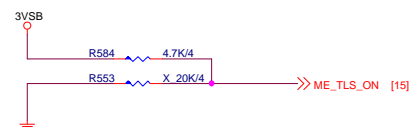
No Reboot



0 : DISABLE (Default)  
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

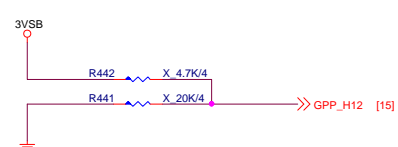
AMT and SBA with confidentiality



0 : DISABLE  
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

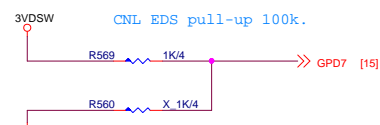
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING  
1 : SLAVE ATTACHED FLASH SHARING

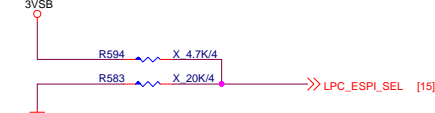
Internal pull-down 20K is disabled after RSMRST

Reserved



XTAL INPUT MODE  
0 = XTAL INPUT IS SINGLE-ENDED  
1 = XTAL INPUT IS DIFFERENTIAL  
PCH HAS INTERNAL 20K PD

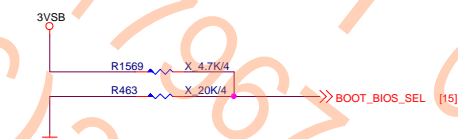
LPC eSPI Mode



0 : LPC  
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Boot BIOS

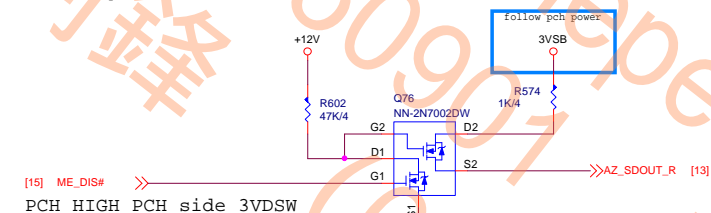


0 : SPI  
1 : LPC

Internal pull-down 20K is disabled after PLTRST#

HDA\_SDO

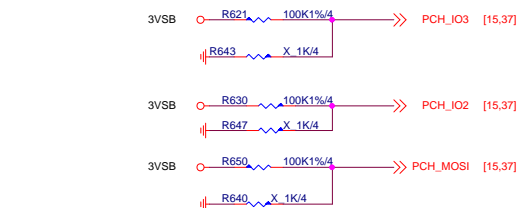
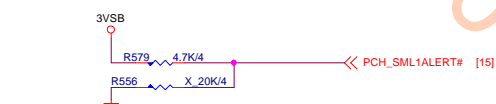
ME flash by GPIO



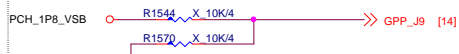
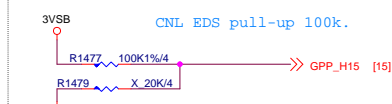
[15] ME\_DIS#

PCH HIGH PCH side 3VDSW

Reserved

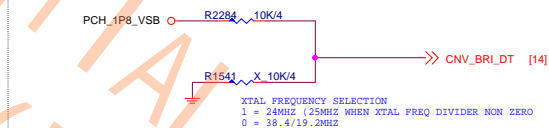


Reserved

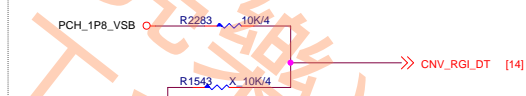


VCCSPI 3.3V, Internal pull-down.

SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE  
0 = VCCSPI IS CONNECTED TO 3.3V RAIL - DEFAULT  
1 = VCCSPI IS CONNECTED TO 1.8V RAIL  
PCH HAS INTERNAL 20K PD



XTAL FREQUENCY SELECTION  
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO  
0 = 38.4/19.2MHZ



An external pull-up or pull-down is required.  
0 = Integrated CNVi enable  
1 = Integrated CNVi disable  
Voltage level - 1.8V only

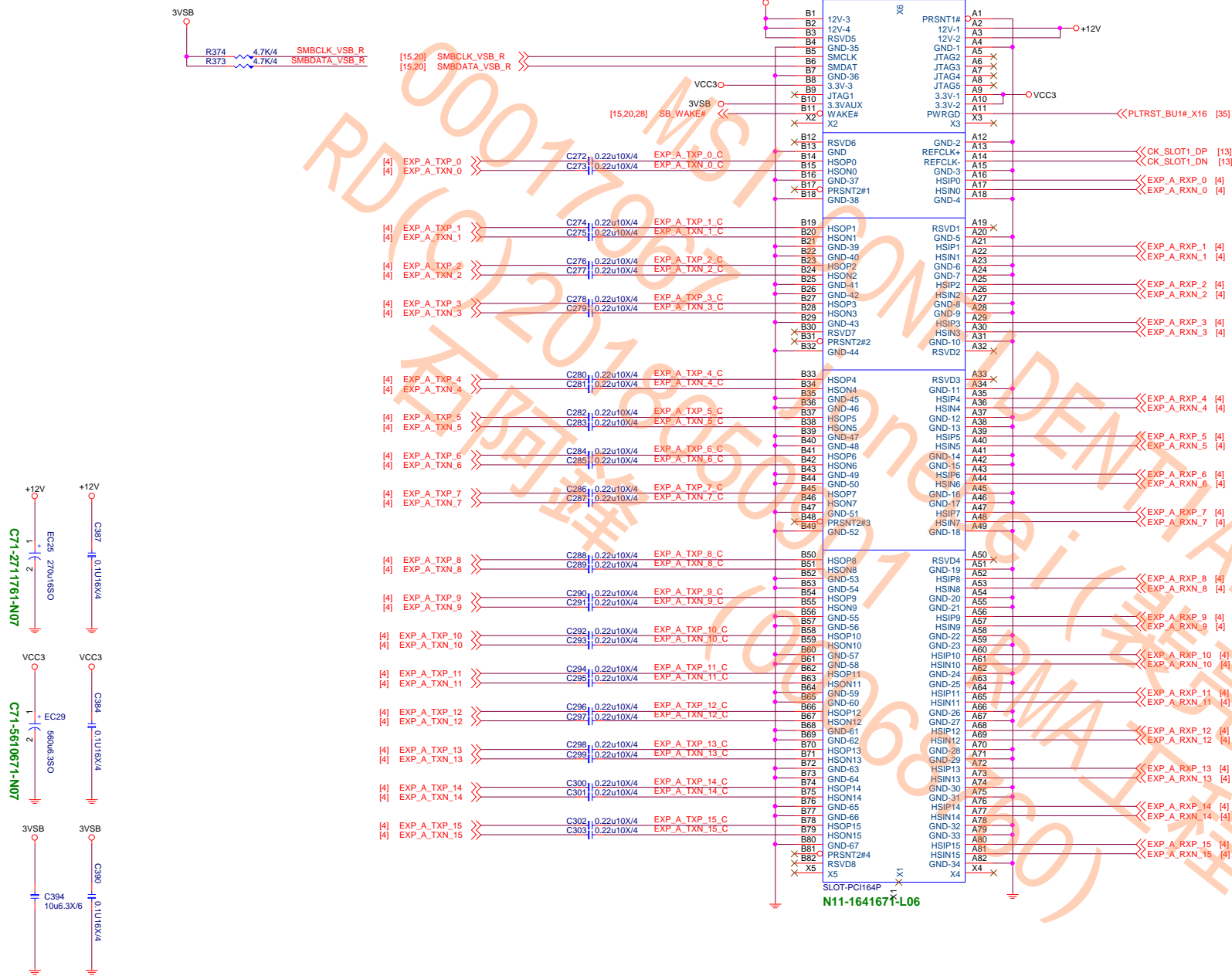


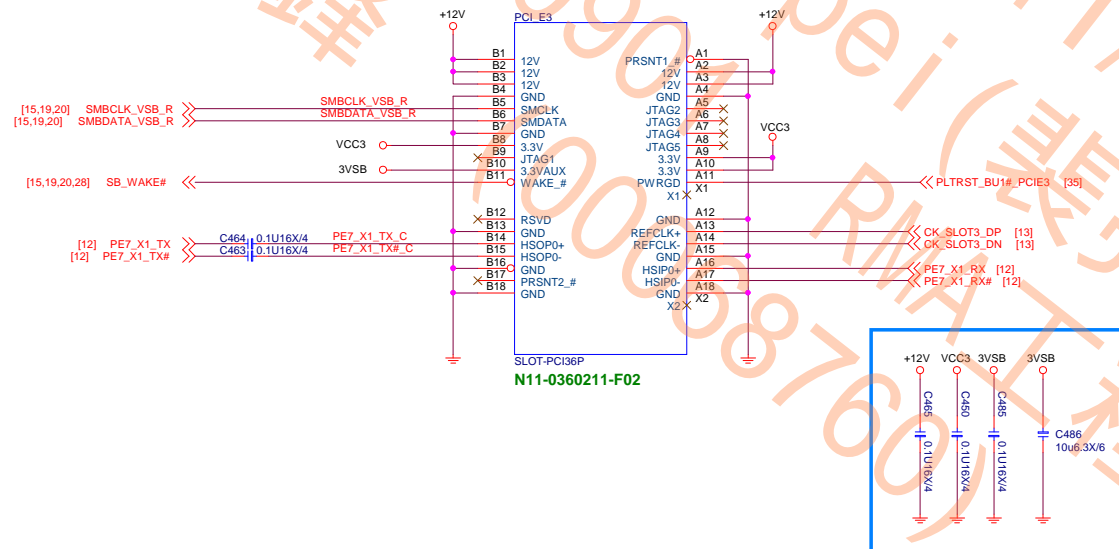
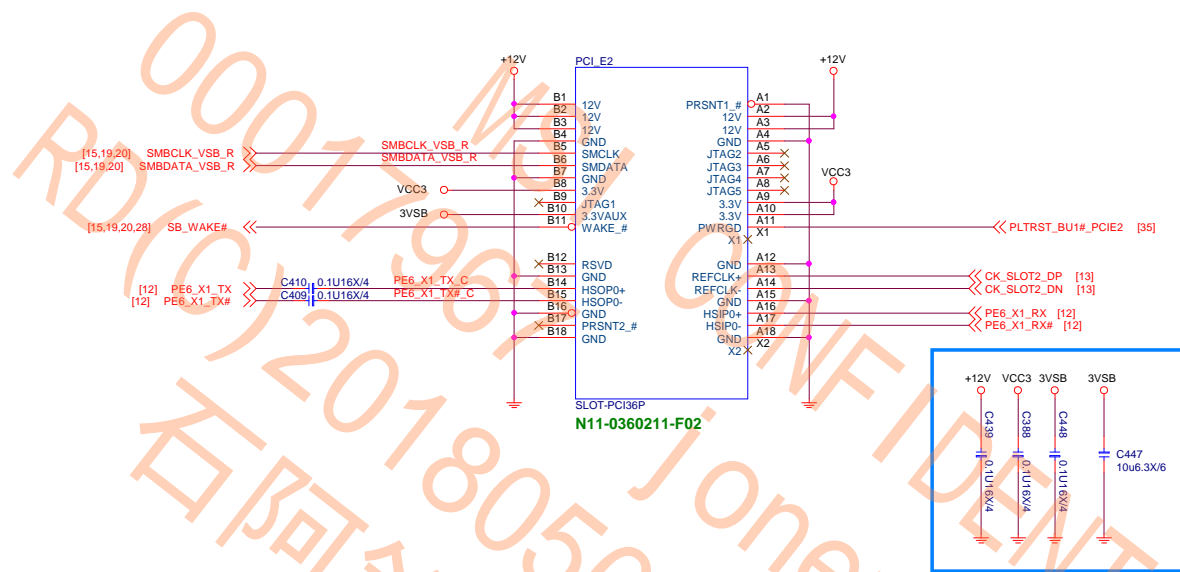
MICRO-STAR INT'L CO.,LTD

MS-7B28

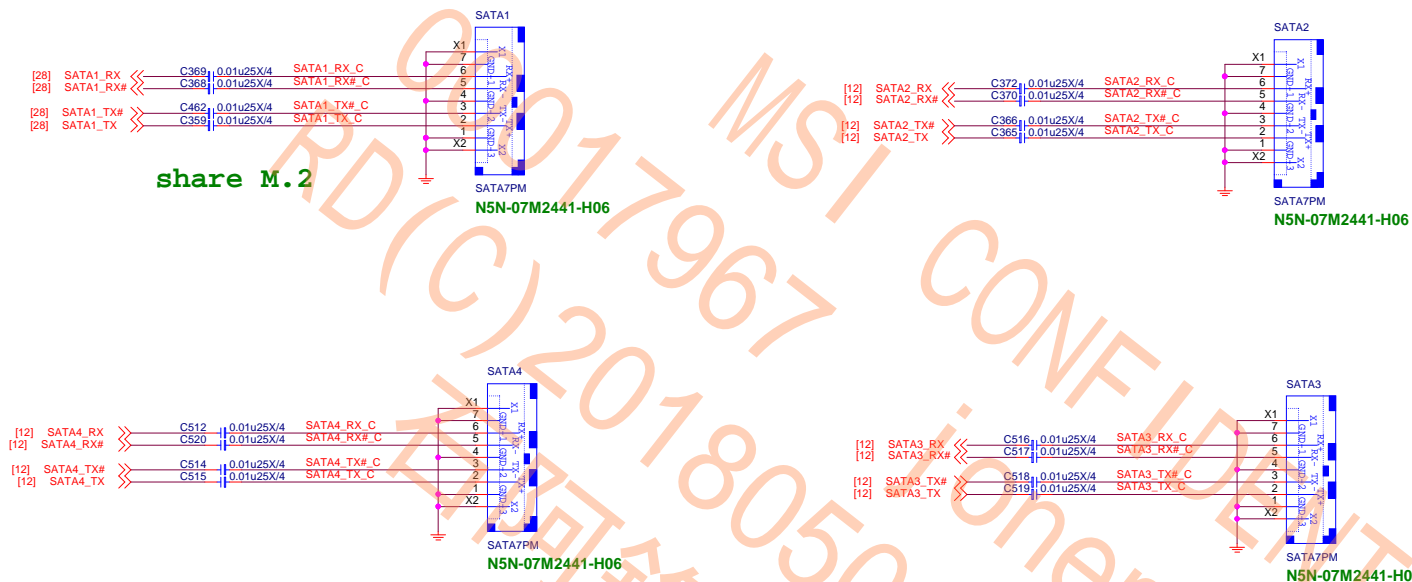
Size	Document Description	Rev
Custom	PCH-Strap	11/2
Date: Friday, January 19, 2018	Sheet 18 of 60	

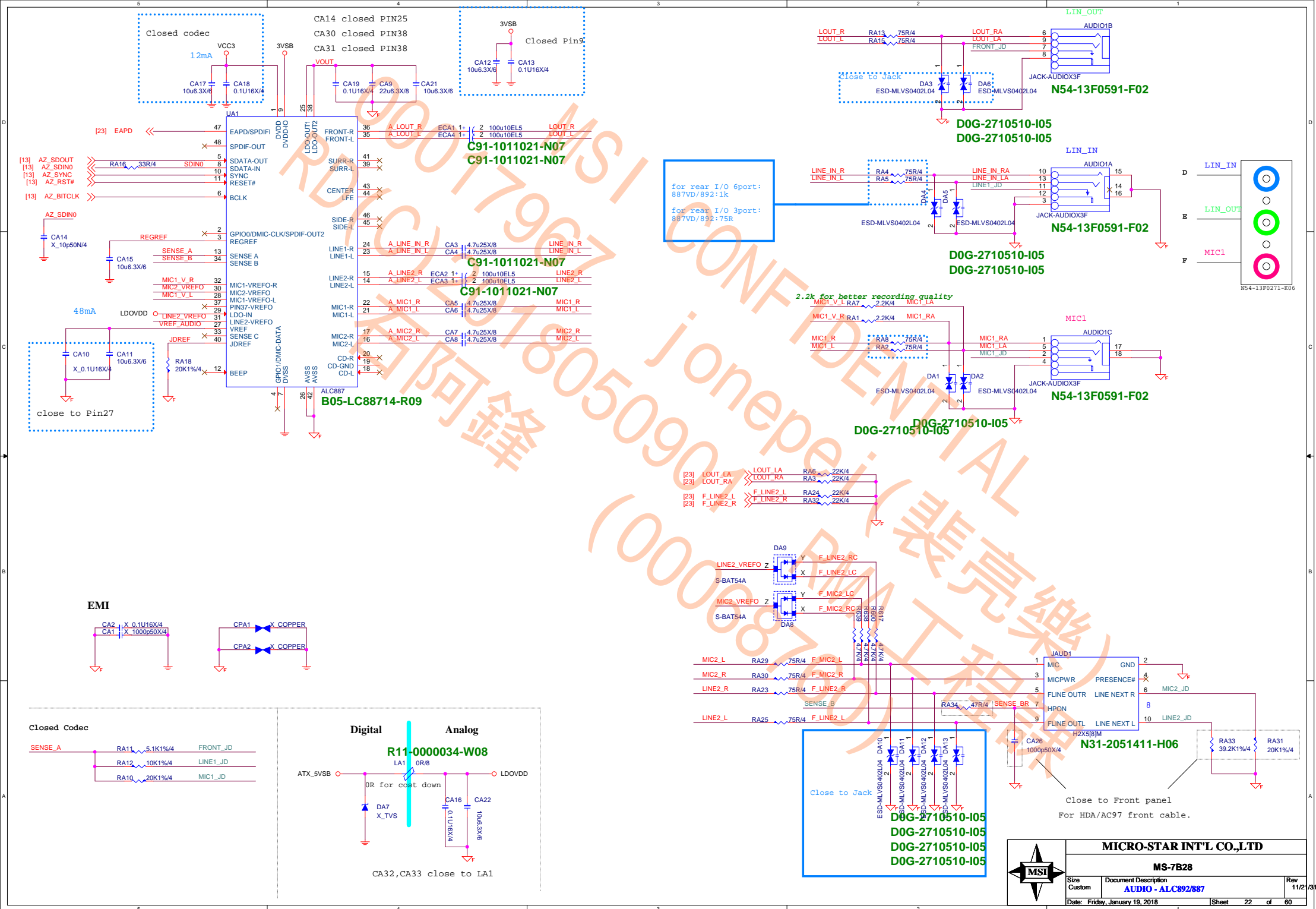






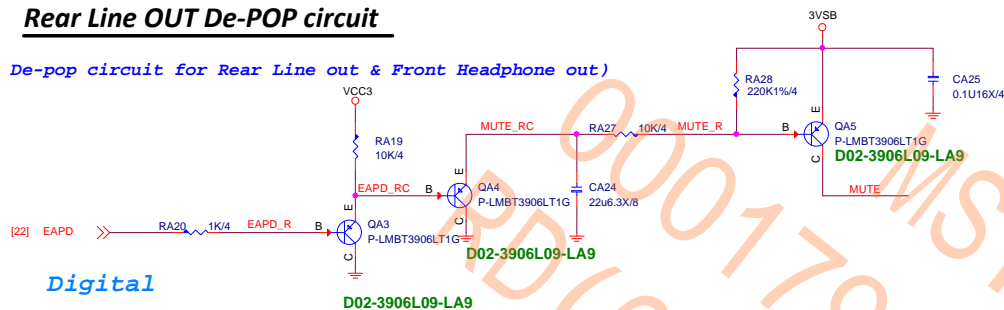
# SATA 6G





### ***Rear Line OUT De-POP circuit***

De-pop circuit for Rear Line out & Front Headphone out)

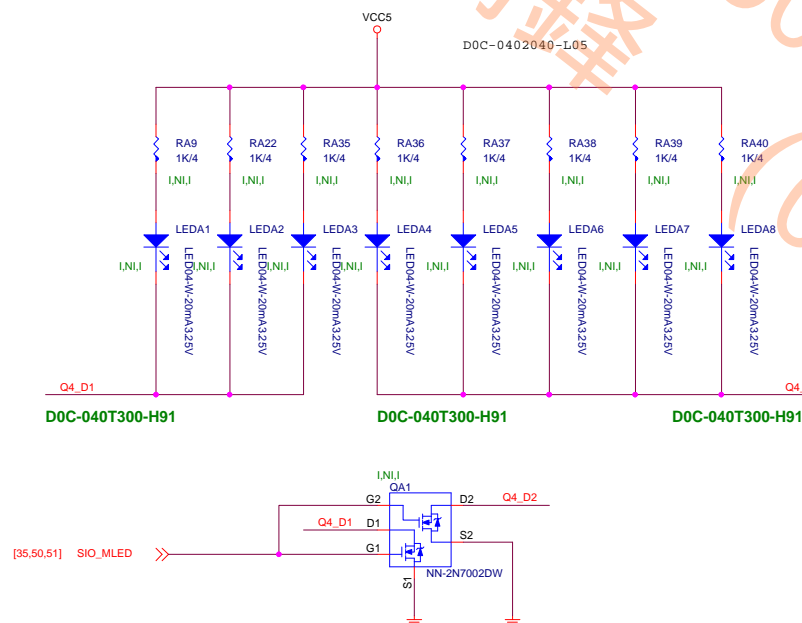


### Analog



Audio moat is transparent and width 40mil

### Audio LED



Schematic Cfg	Project	
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V	C



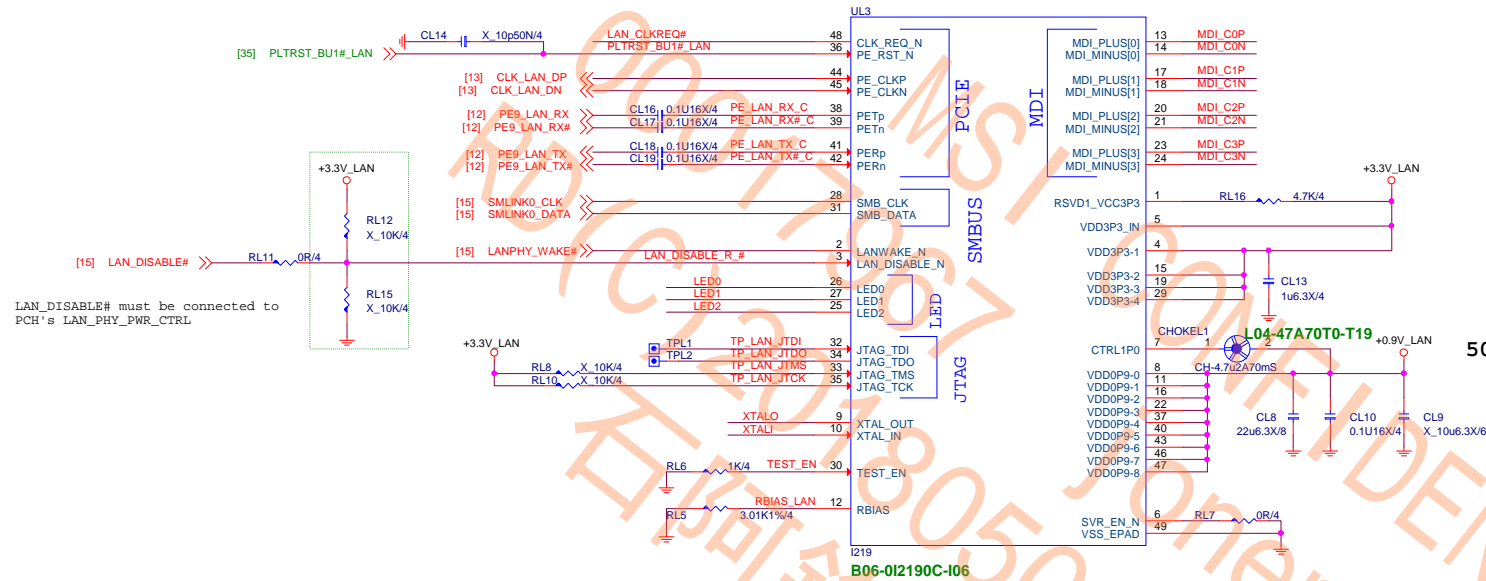
**MICRO-STAR INT'L CO.,LTD**

MS-7B28

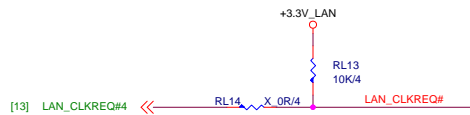
Size Custom	Document Description <b>AUDIO - depop circuit</b>	Rev 11/2/3
Date: Friday, January 19, 2018		Sheet 23 of 60



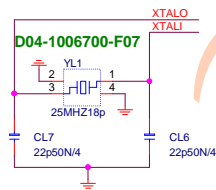
Intel Lan- I219



PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.  
If CLK\_REQ\_N is not used, pin48 is pulled up 10KR to 3.3V\_LAN

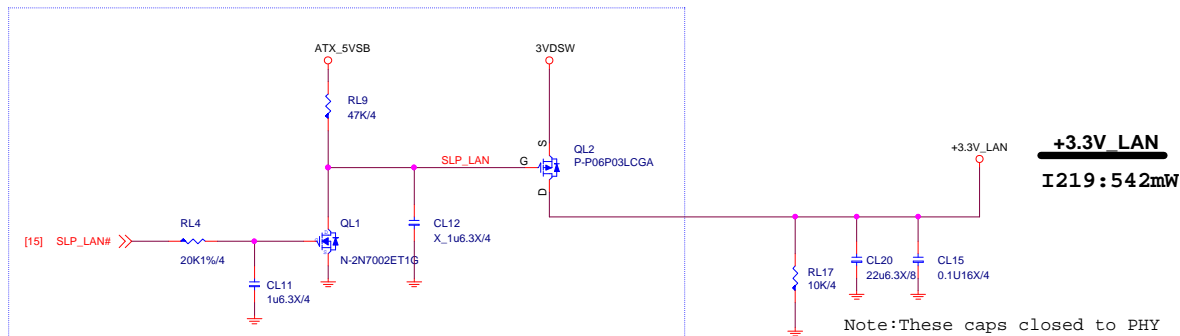


AVL:D04-1005700-SC6

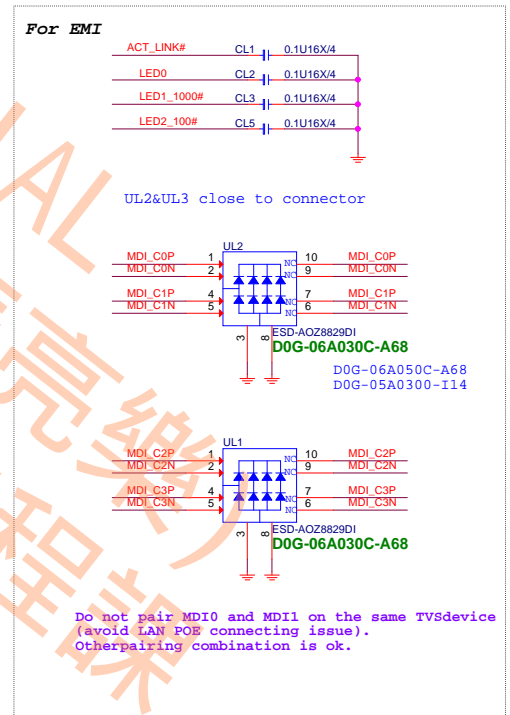
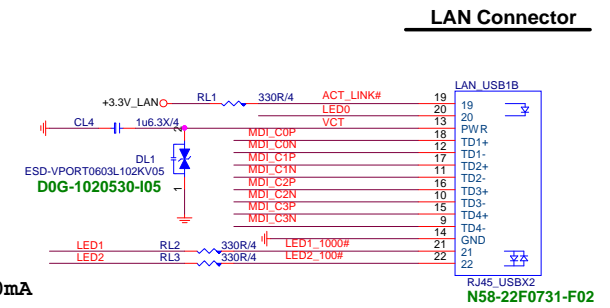


The 10Kohm pull-up resistor (RL18) of CLK\_REQ\_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:  
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



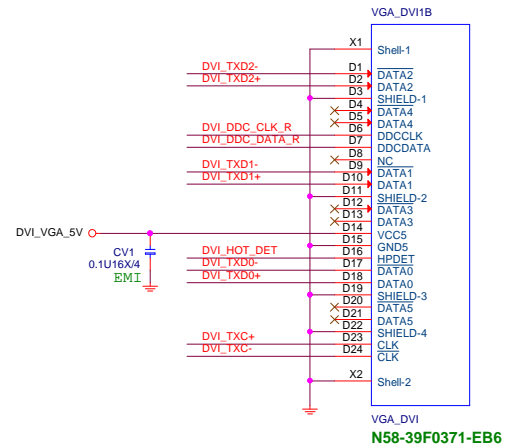
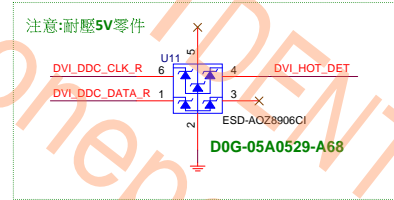
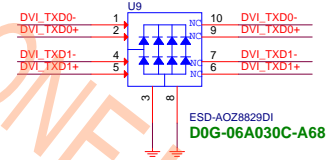
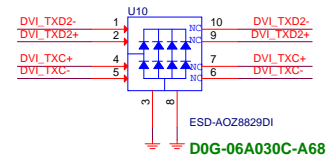
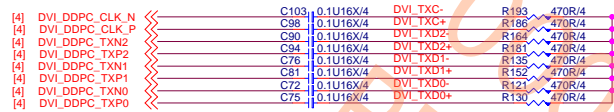
Note: These caps closed to PHY



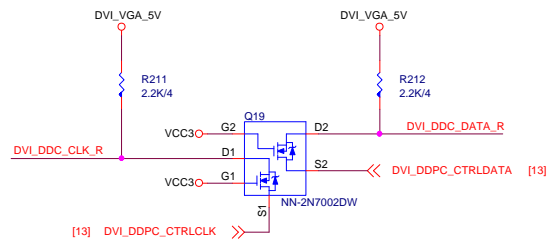
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7B28</b>		
Size Custom	Document Description <b>LAN - I219</b>	Rev 11/2
Date: Friday, January 19, 2018	Sheet 24	of 60

# DVI level shifter

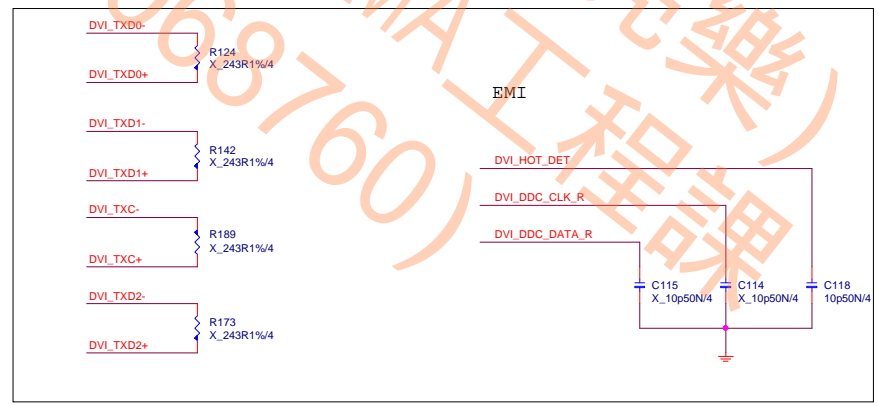
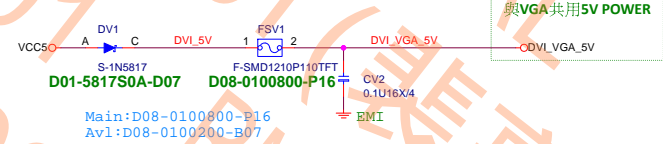
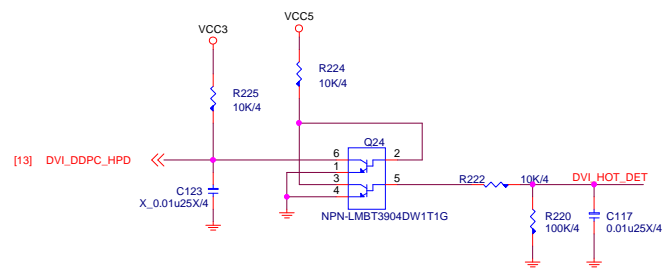
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



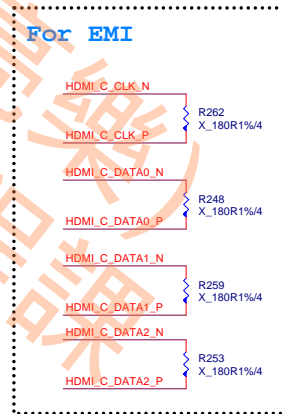
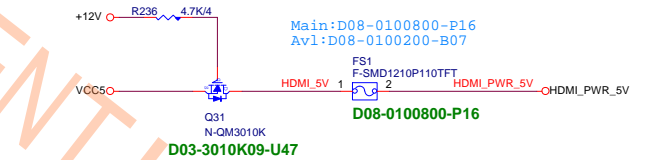
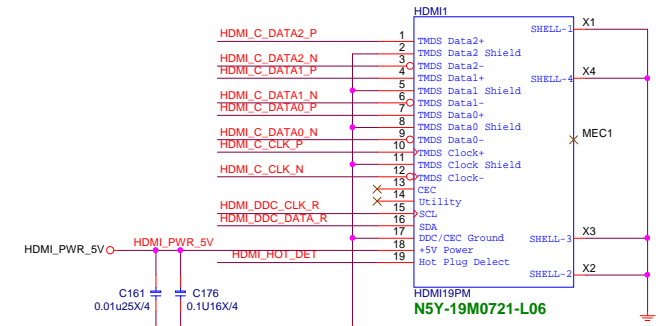
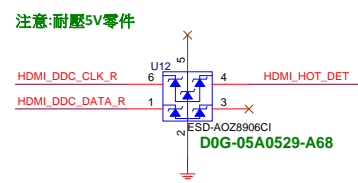
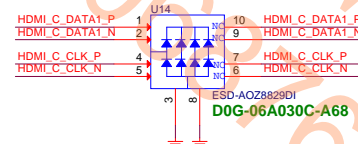
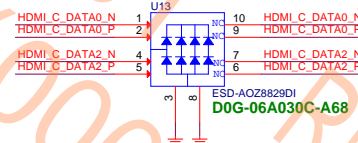
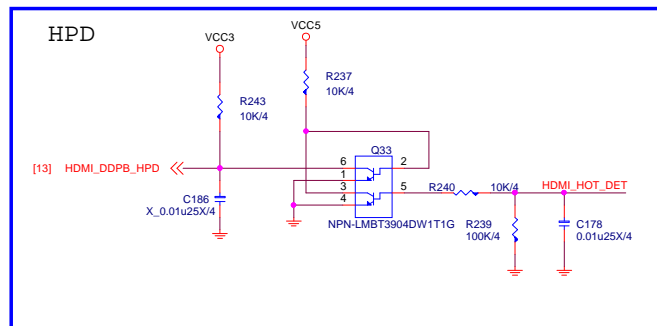
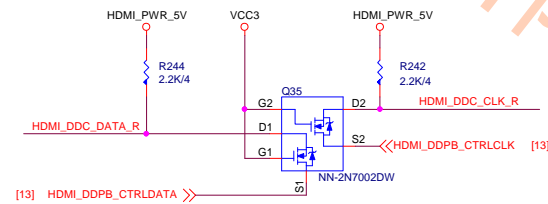
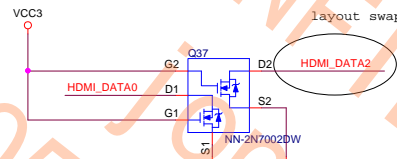
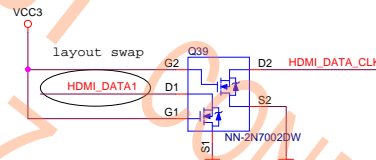
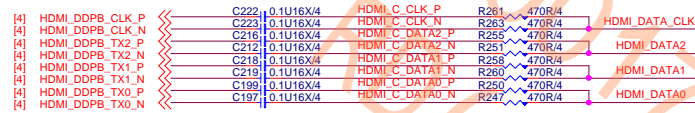
## LEVEL SHIFT using I2C Repeater



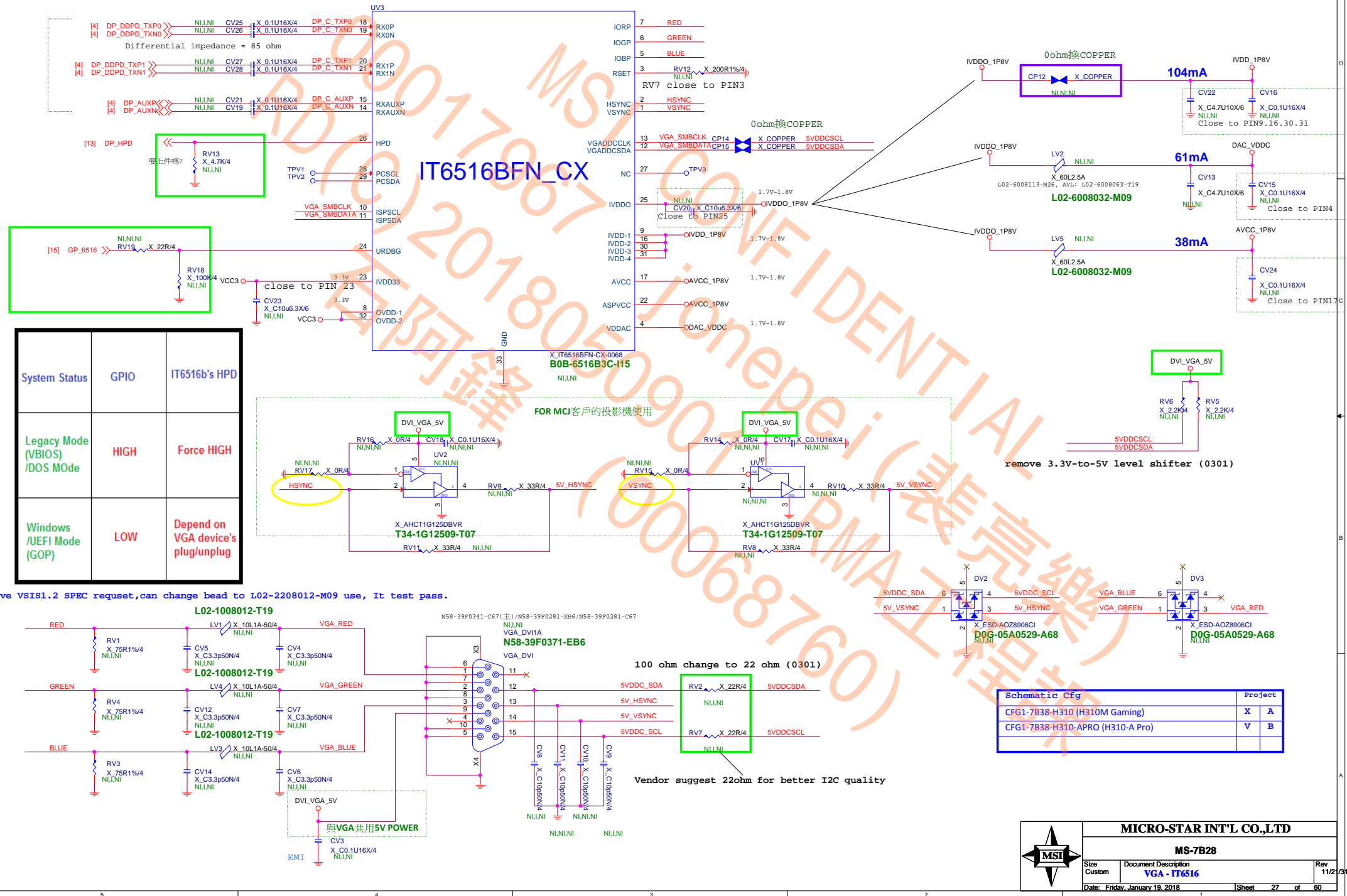
## HPD

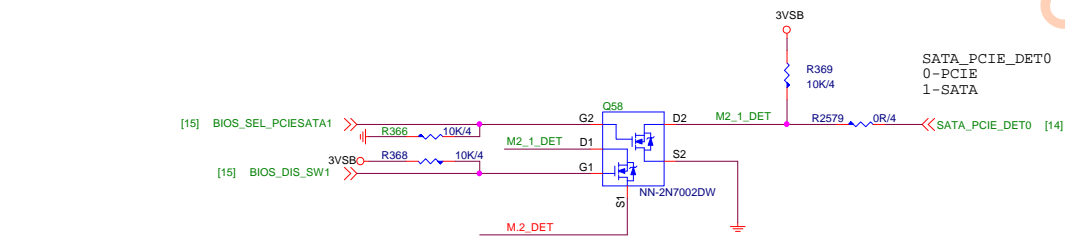
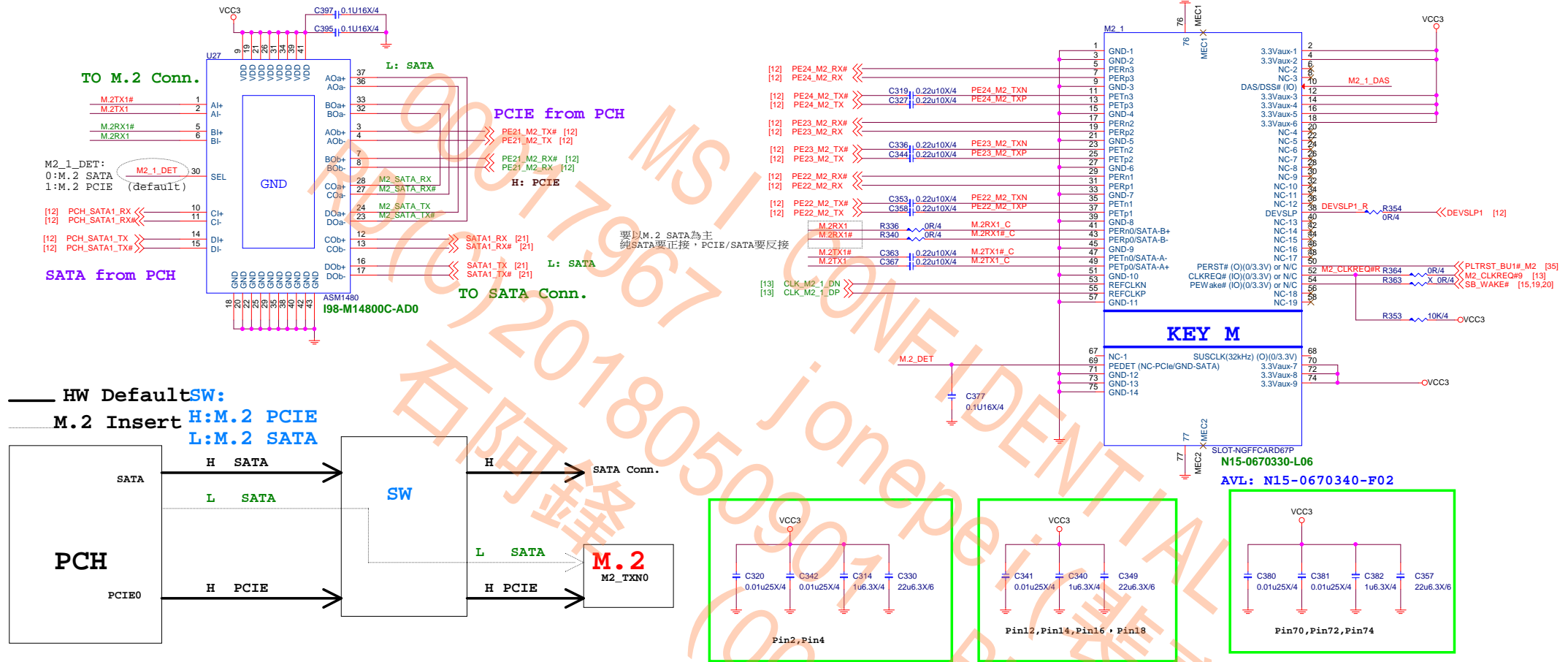


HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

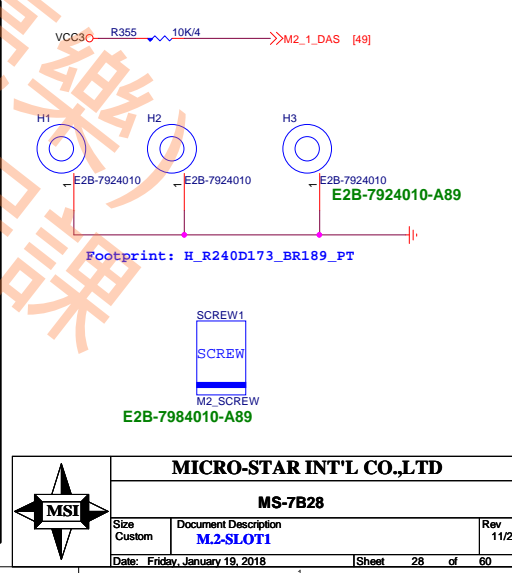


**Note:**  
If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining



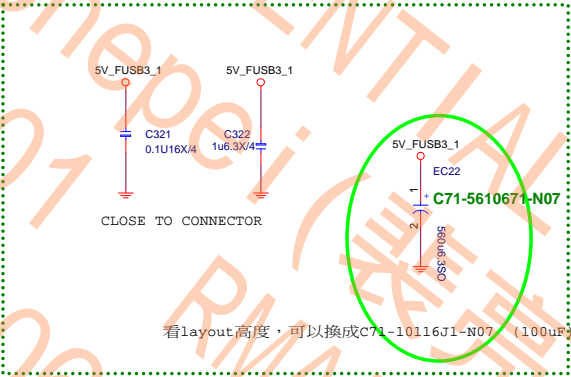
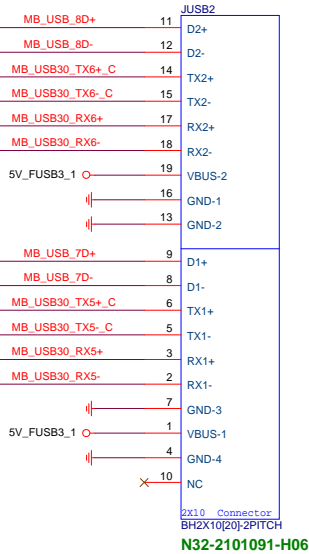
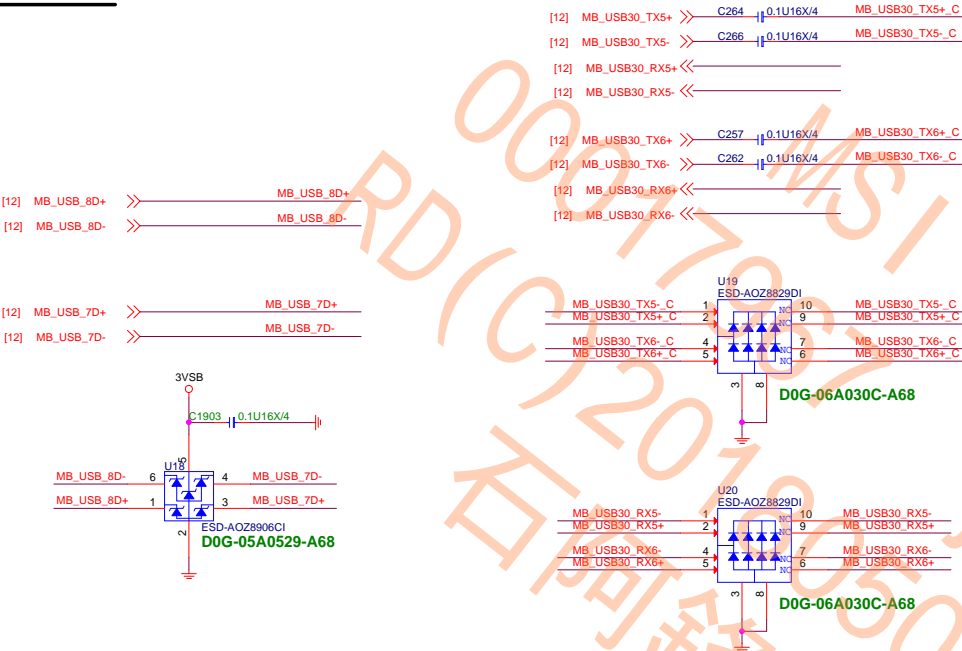


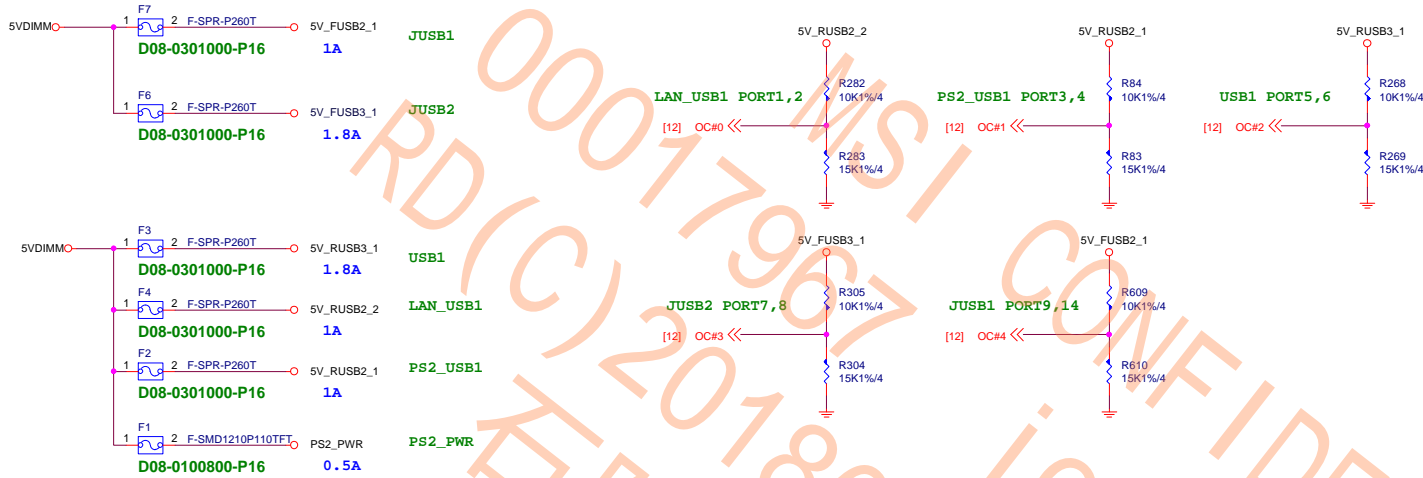
GPP_H14	GPP_H13	BIOS_MODE
BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO





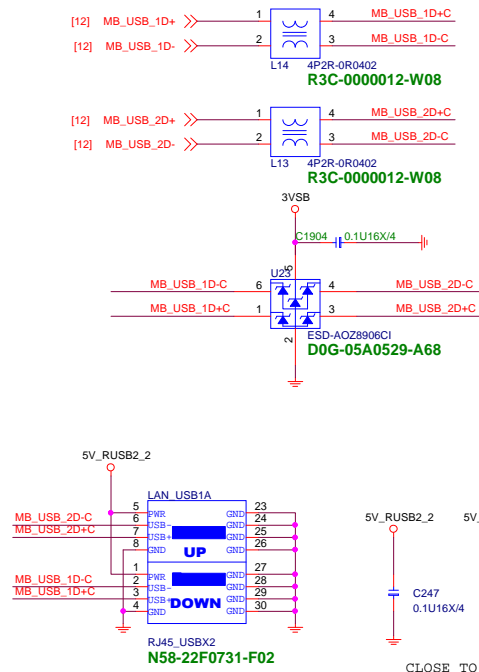
Front JUSB3 port 7,8



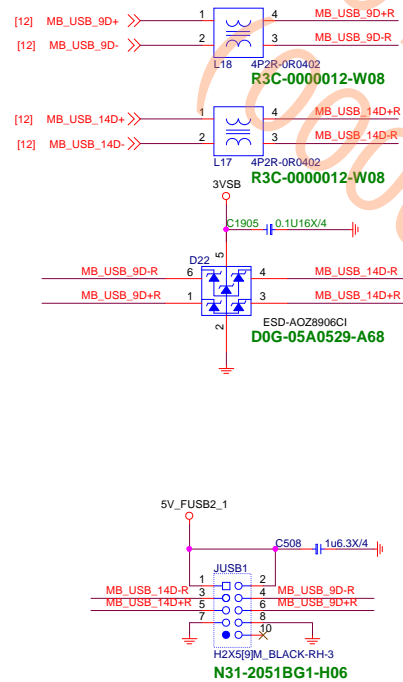


USB CONN	USB POWER	PCH PORT	OC# SIGNAL
LAN_USB1	5V_RUSB2_2	Port1,2	OC#0
PS2_USB1	5V_RUSB2_1	Port3,4	OC#1
USB1	5V_RUSB3_1	Port5,6	OC#2
JUSB2	5V_FUSB3_1	Port7,8	OC#3
JUSB1	5V_FUSB2_1	Port9,14	OC#4

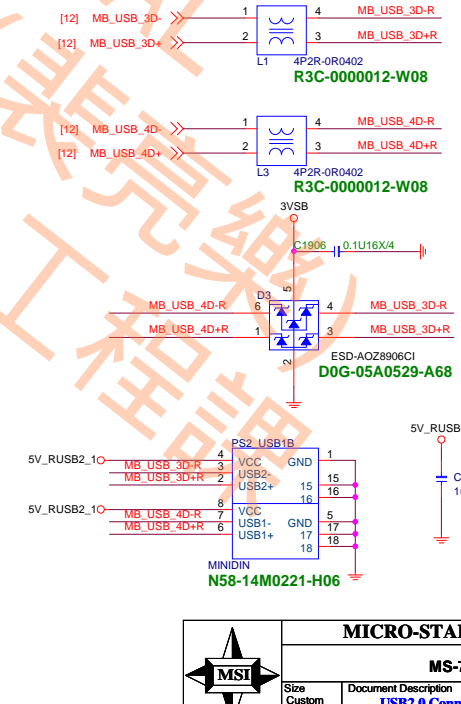
#### Rear USB1 port 1,2



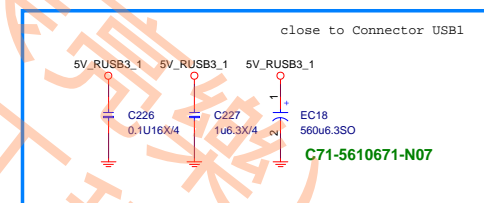
#### JUSB1 PORT 9,14



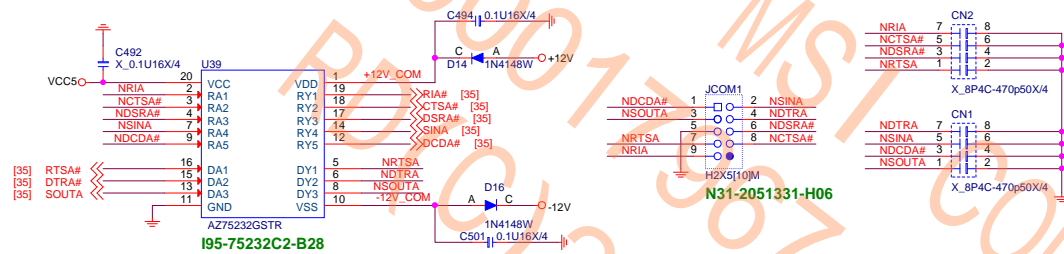
#### PS2\_USB1 PORT 3,4



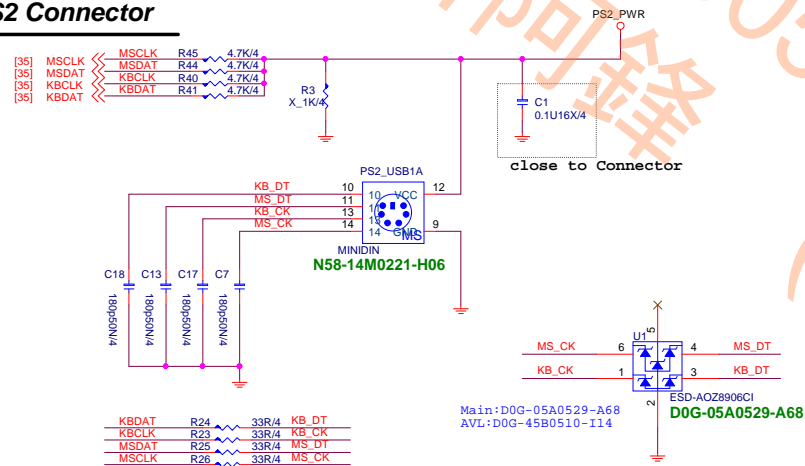
MICRO-STAR INT'L CO.,LTD			
MS-7B28			
Size	Document Description	Rev	
Custom	USB2.0 Connector	11/2	
Date: Friday, January 19, 2018		Sheet	30 of 60

[illegible]

## SERIAL PORT 1



### PS2 Connector

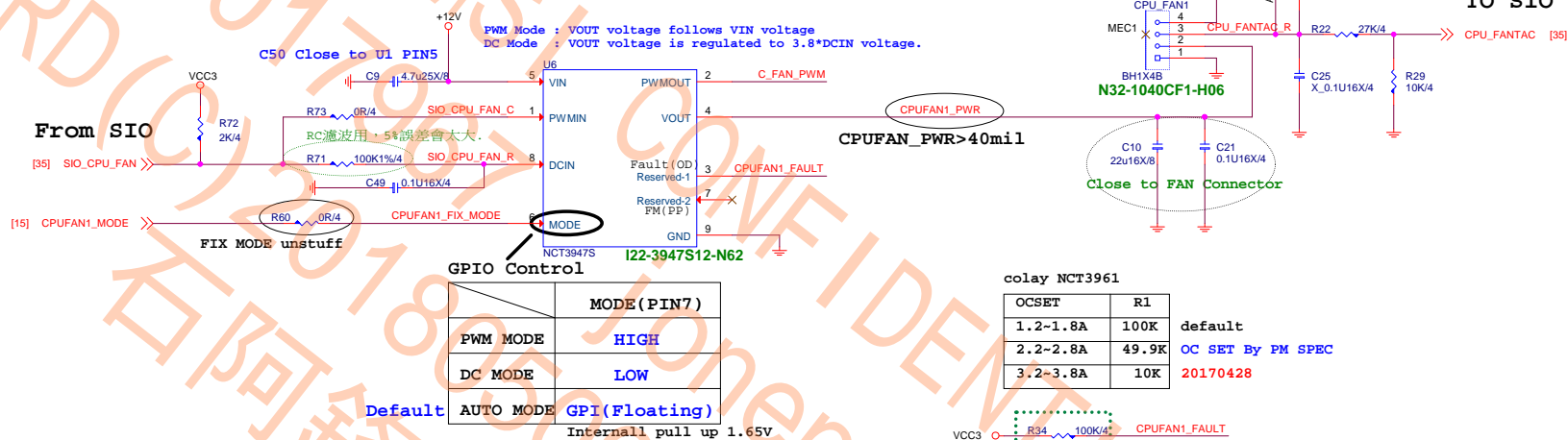


**MICRO-STAR INT'L CO.,LTD**

MS-7B28

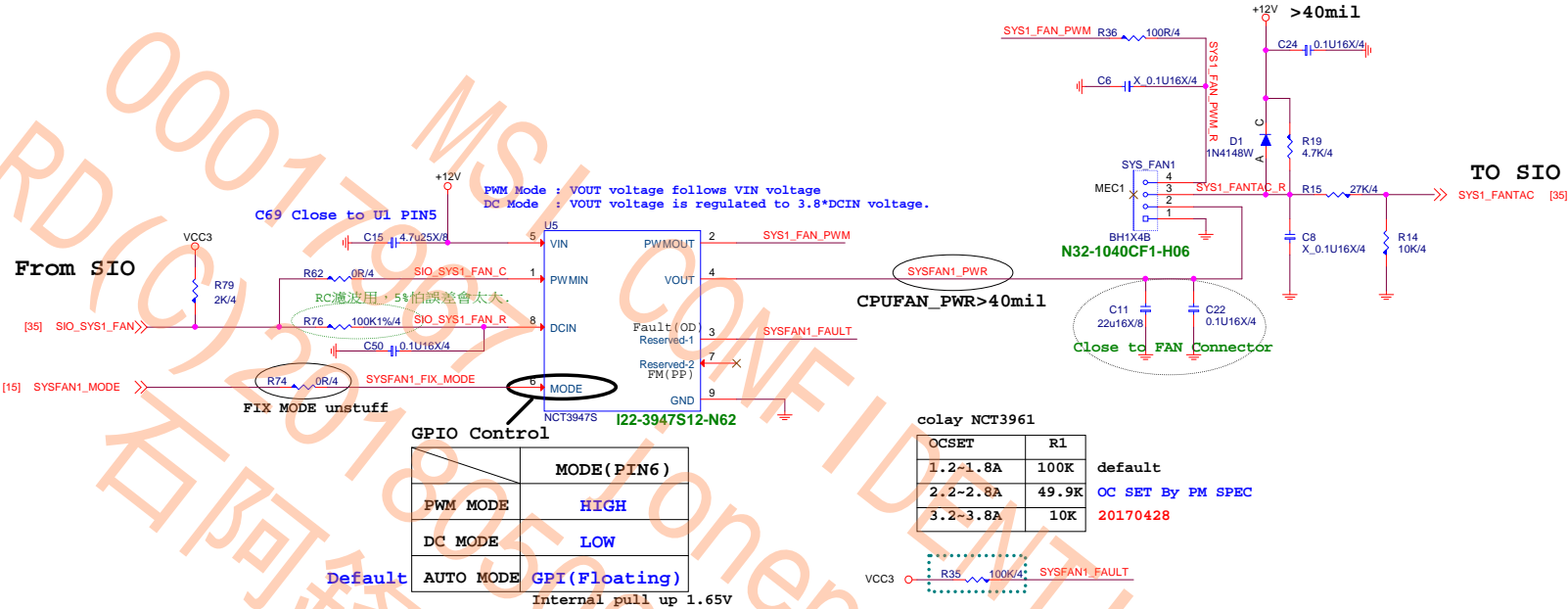
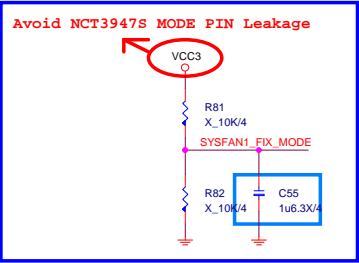
Size Custom	Document Description <b>SERIAL POR/PS2</b>	Rev 11/2/31
Date: Friday, January 19, 2018		Sheet 32 of 60

## GPIO可以由BIOS切換 PWM/DC MODE

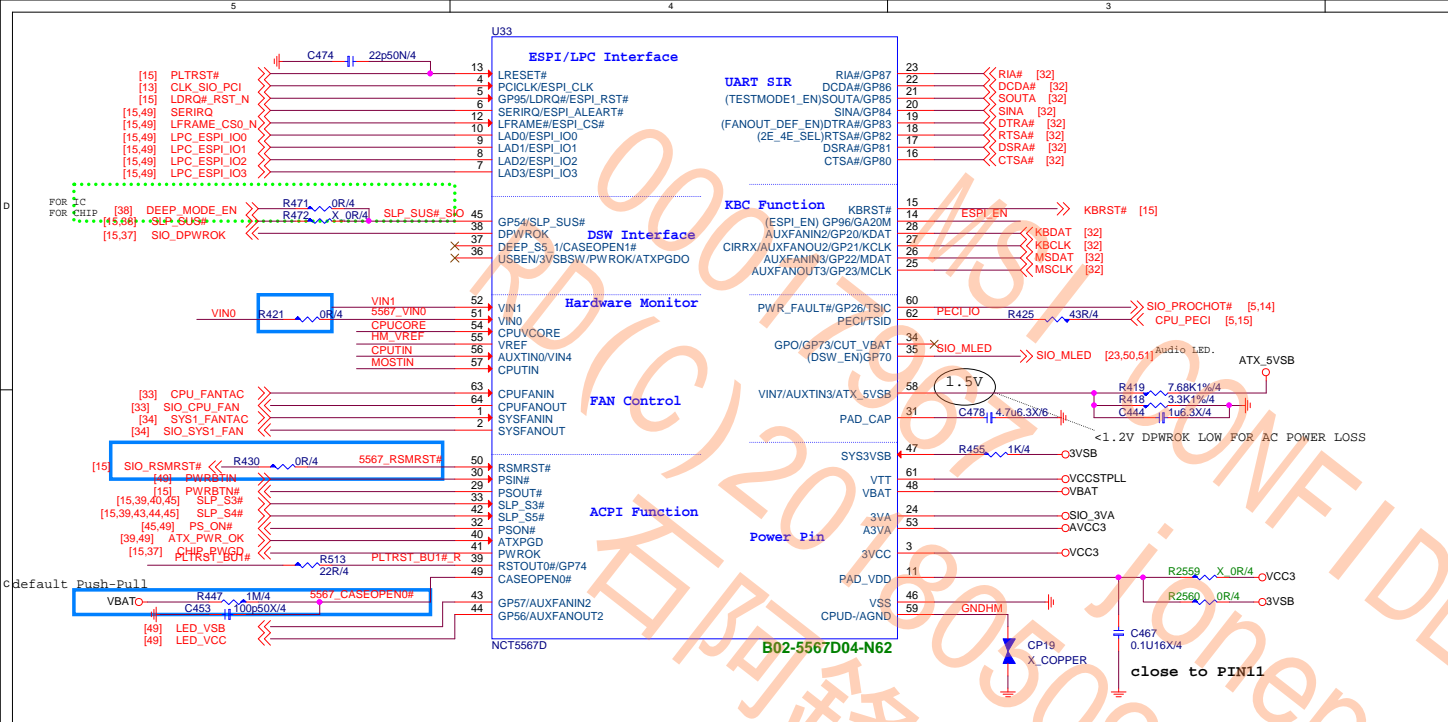


OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

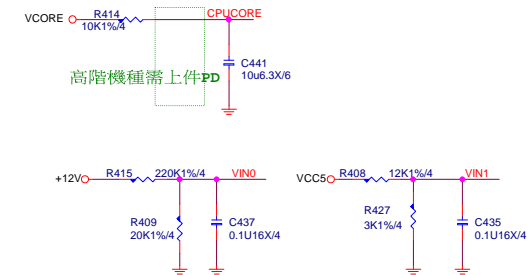
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE





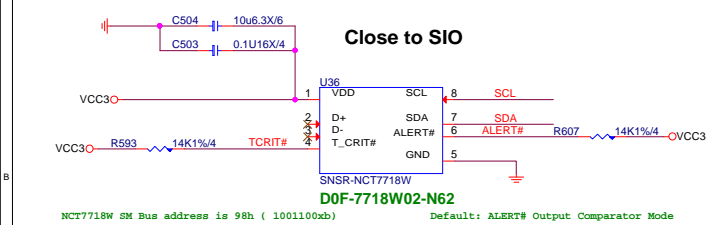


## HW Monitor - Voltage



PIN	5567D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TESTMODE	ENABLE TESTMODE
14	ESPI_EN	GA20M	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	DISABLE	ENABLE DSW_EN

## NCT7718W



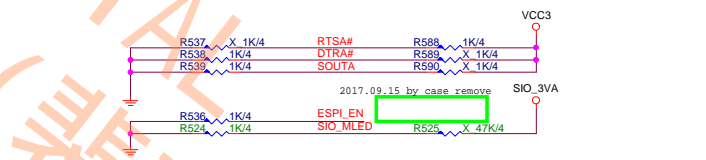
Please Make Sure Your SM Bus is Pull-Up to VCC3

SMBCLK\_VCC [8.15] SMBDATA\_VCC [8.15]

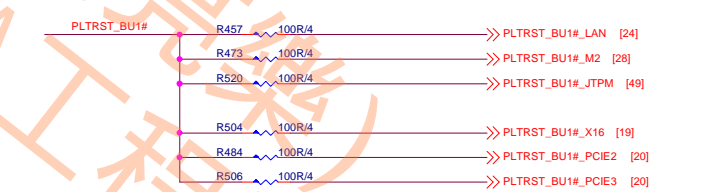
C客值要上很小才不會引到掉機

TEMPERATURE (°C)	2KQ	7.5KQ	10.5KQ	14KQ	18.7KQ
7.5KQ	77	87	97	107	117
10.5KQ	81	91	101	111	121
14KQ	83	93	103	113	123
18.7KQ	85	95	105	115	125

ALERT#



need near SIO

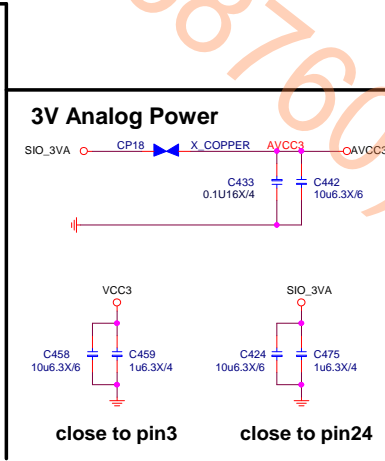
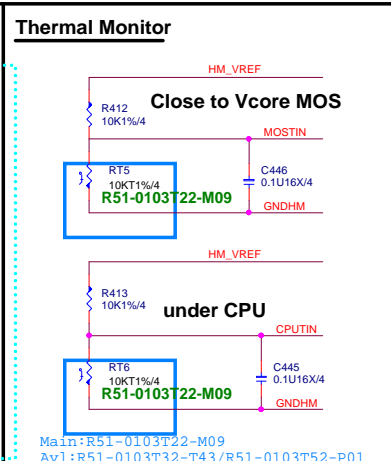
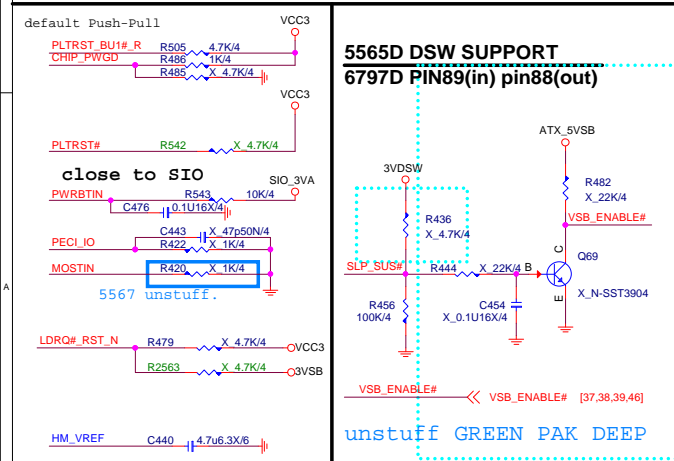


5567 colay 5565.

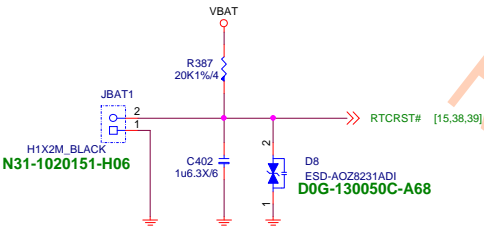
5567 Pin51	5565 Pin51
5567_VIN0	R428 X_0R/4 VIN1
5567 Pin50	5565 Pin50
5567_RSMRST#	R429 X_0R/4 VIN0
5567 Pin49	5565 Pin49
5567_CASEOPEN0#	R440 X_0R/4 SIO_RSMRST#



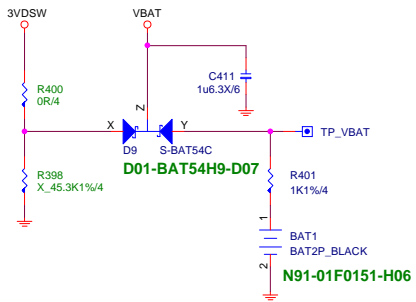
MICRO-STAR INT'L CO.,LTD		
MS-7B28		
Size	Document Description	Rev
Custom	SIO NCT6797-1	11/2
Date: Friday, January 19, 2018	Sheet 35 of 60	



Cut VBAT

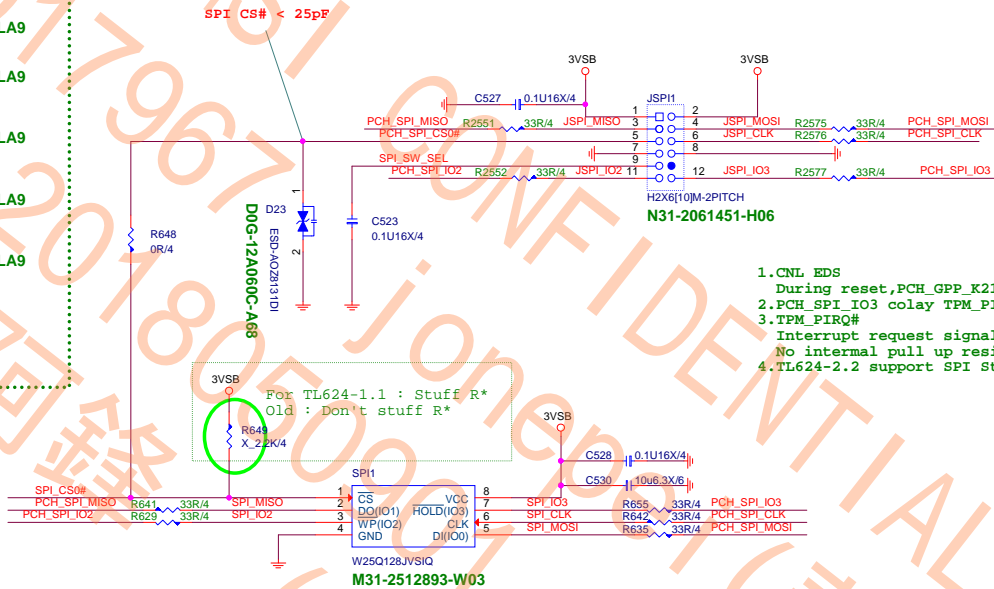
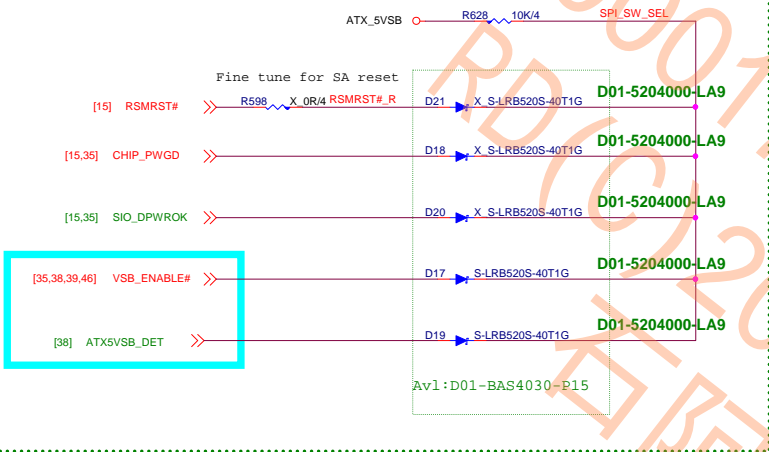


VBAT



[15]	PCH_SPI_CS0#	<<	PCH_SPI_CS0#
[15,18]	PCH_MOSI	<<	R2546 0R/4 PCH_SPI_MOSI
[15]	PCH_MISO	<<	R2547 0R/4 PCH_SPI_MISO
[15]	PCH_CLK	<<	R2548 0R/4 PCH_SPI_CLK
[15,18]	PCH_IO2	<<	R2549 0R/4 PCH_SPI_IO2
[15,18]	PCH_IO3	<<	R2550 0R/4 PCH_SPI_IO3

stuff TL624 SPI\_SW\_SEL pull low, 左邊的訊號會拉low, 提供VSB for TL624.



- 1.CNL EDS  
During reset,PCH\_GPP\_K21 via 20k pull up to 3.3V.
- 2.PCH\_SPI\_IO3 colay TPM\_PIRQ#(1.8V or 3.3V,OD)
- 3.TPM\_PIRQ#  
Interrupt request signal to the host.  
No internal pull up resistor.Active low.
- 4.TL624-2.2 support SPI Standard Mode.

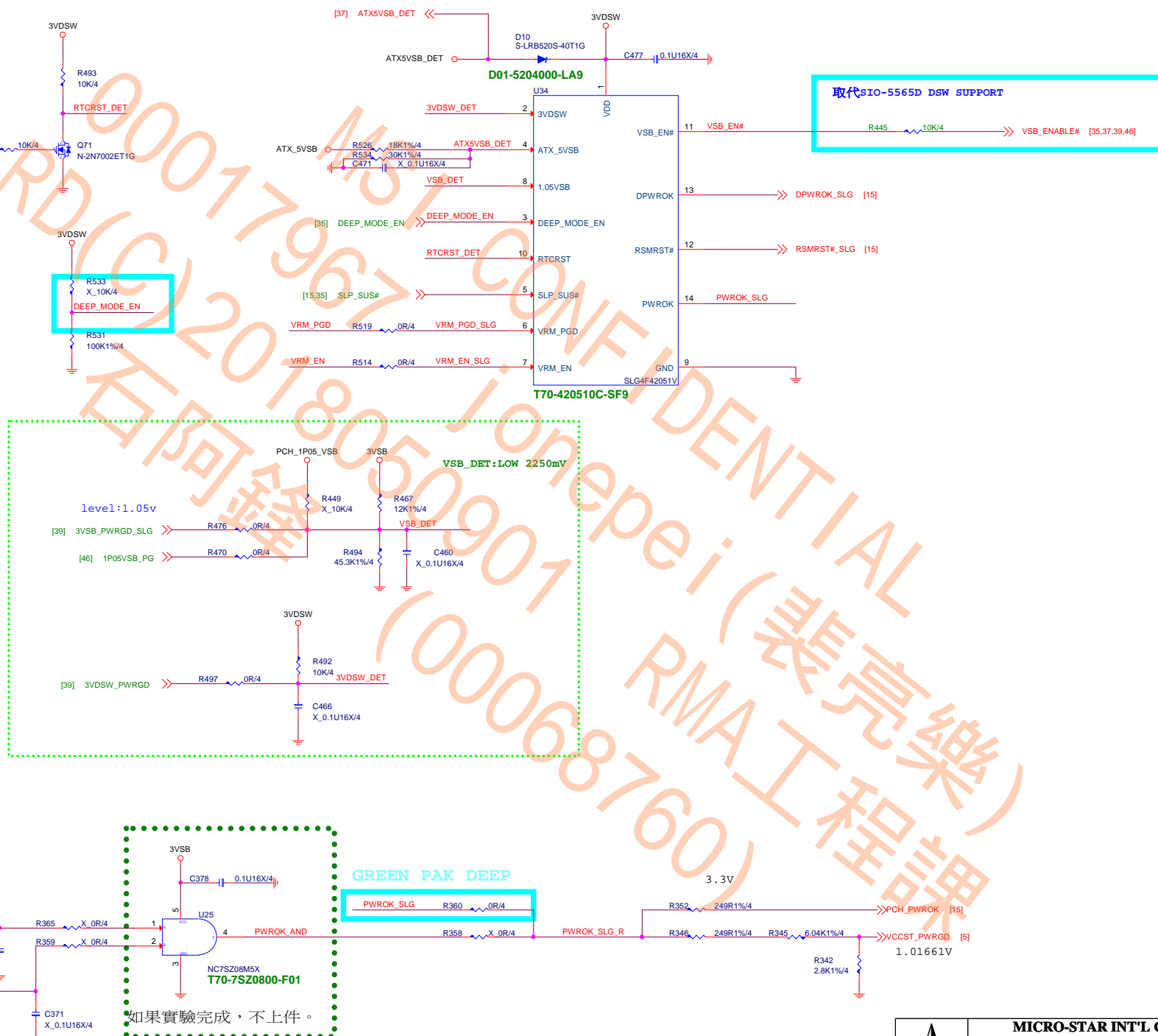


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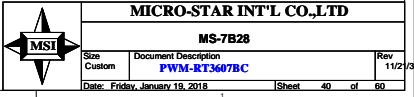
Size Custom	Document Description BIOS ROM	Rev 11/2
Date: Friday, January 19, 2018	Sheet 37 of 60	

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

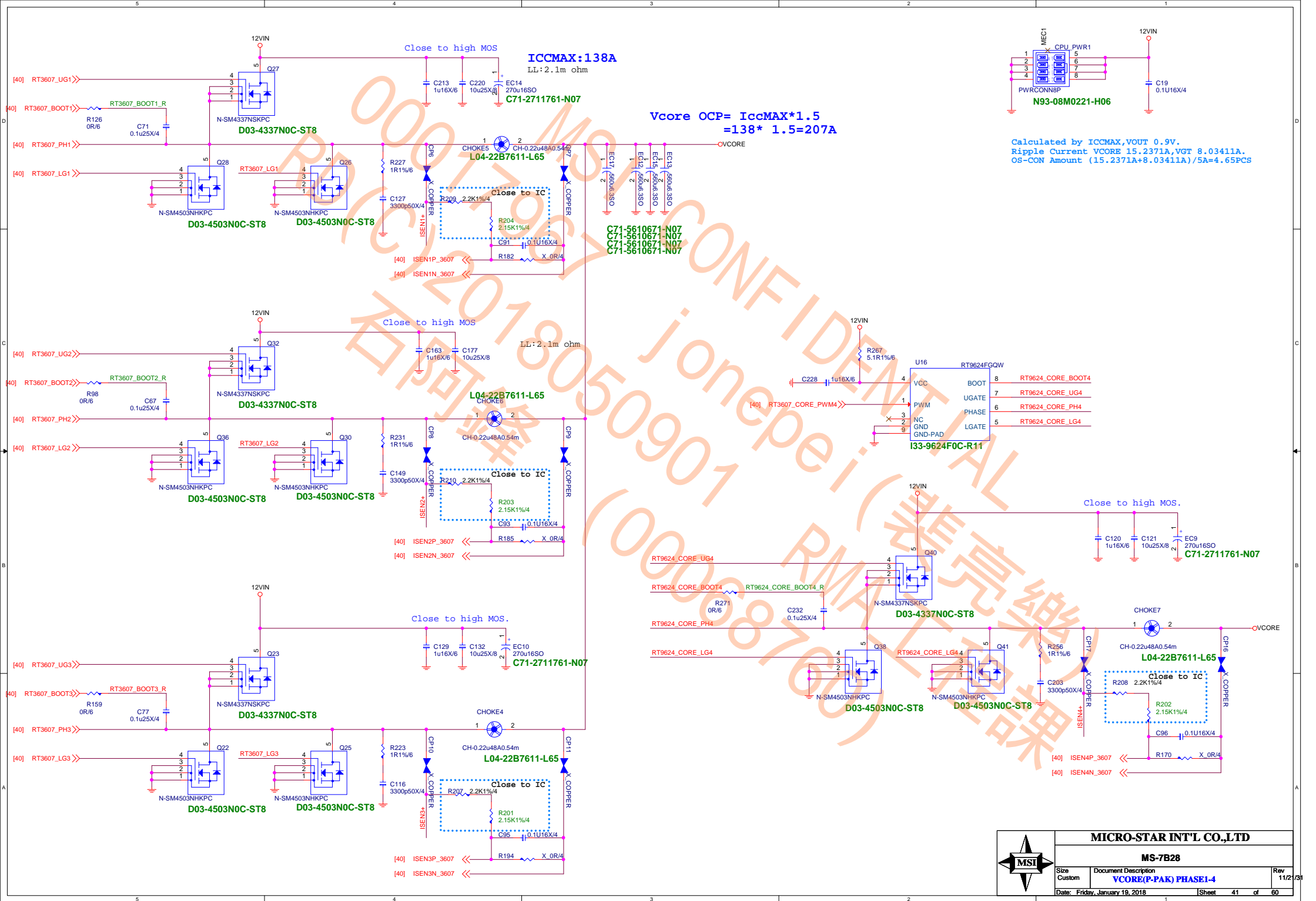


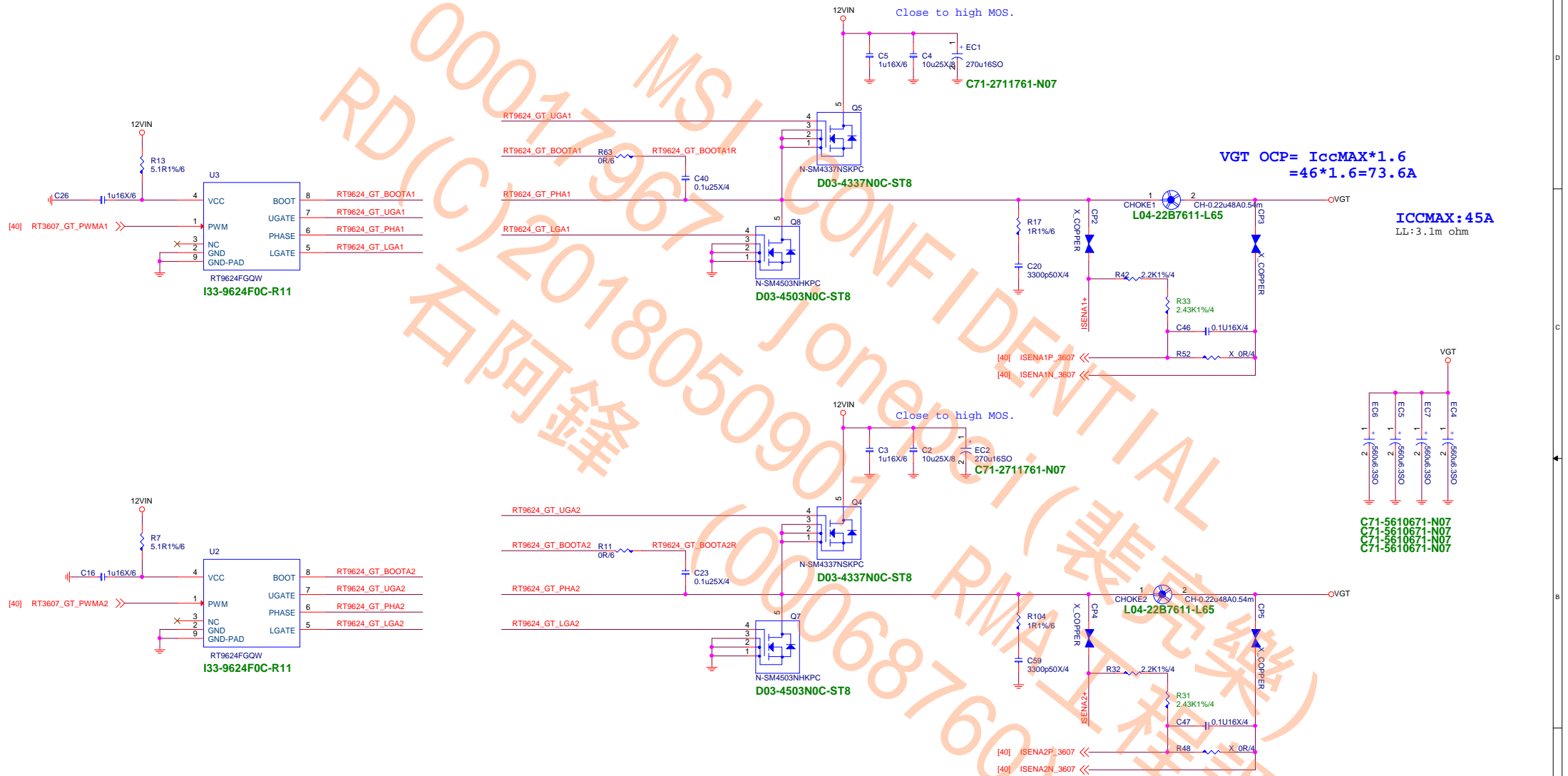
MICRO-STAR INT'L CO.,LTD		
MS-7B28		
Size	Document Description	Rev
Custom	GREEN PAK DEEP	11/2
Date: Friday, January 19, 2018	Sheet 38 of 60	











VCC\_DDR@1.2V/11.525A

DDR4\_1.2V 3.3A+ 7.85A+0.375A=11.525A

3.3A FOR CPU  
10A FOR 2DIMM DDR4  
0.375A FOR VTT\_DDR

Rlimit = Llimit \* Rds \* 10 /5uA

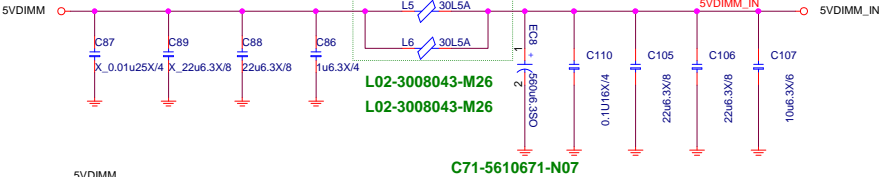
Rlimit = 14.9825\*4\*10/5

D03-632BA0C-N03  
Current limit= 118K\*5uA/10/4mohm=14.75A

0.4V<=Rlimit \*5uA<=3V

VID	Reference Voltage (V)
H	0.675
L	0.75

Input Current= (11.525A\*1.2V)/5V/0.8=3.4575A  
L02-3008043-M26  
Over 85°C ,Rated Current 1.5A.

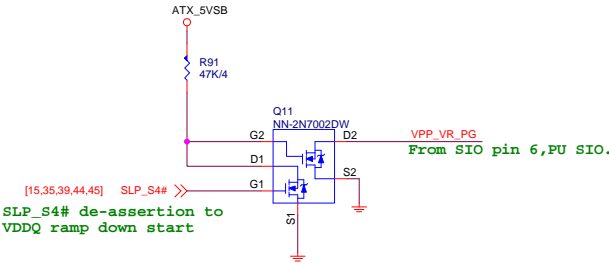


Irms = Iout \* SQRT((Vout/Vin) \* (1-(Vout/Vin)))  
=11.525\* 0.427  
= 4.921175A

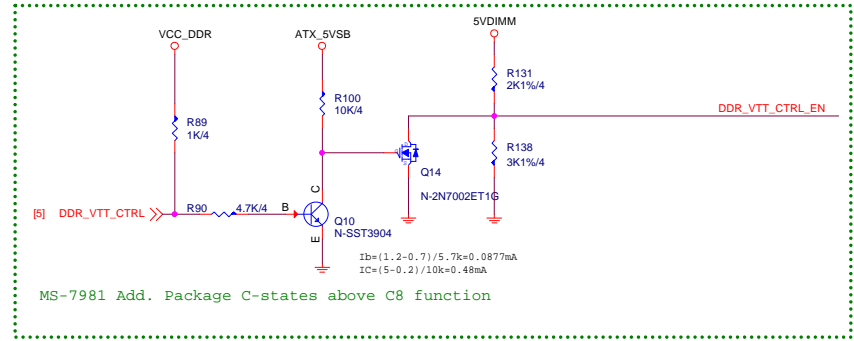
DDR OCP= R44\*5uA/10/Dds(on)  
138k\*5uA/10/3m=23A  
138k\*5uA/10/4.6m=15A  
MOS Rds(on)是3m~4.6m ohm

VTT 固定2.6A  
Current Limit 2.6A

Vout = Vref \* (1 +(R1/R2))  
= 0.75 \* (1 +(1K/1.65K))  
= 1.204V

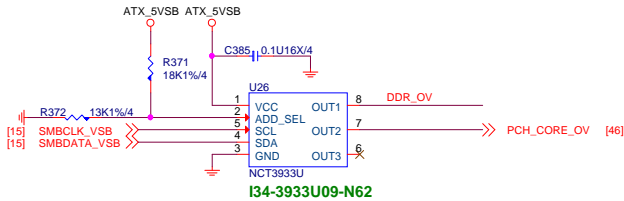


VPP ramp down after VDDQ ramp down



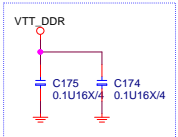
UPI VOLTAGE CONSOLE

0x26 :RH=18K,RL=13K



MAX:11.525A  
1.2V

0.1uFx1 per dimm



DDR VPP 固定4.8A

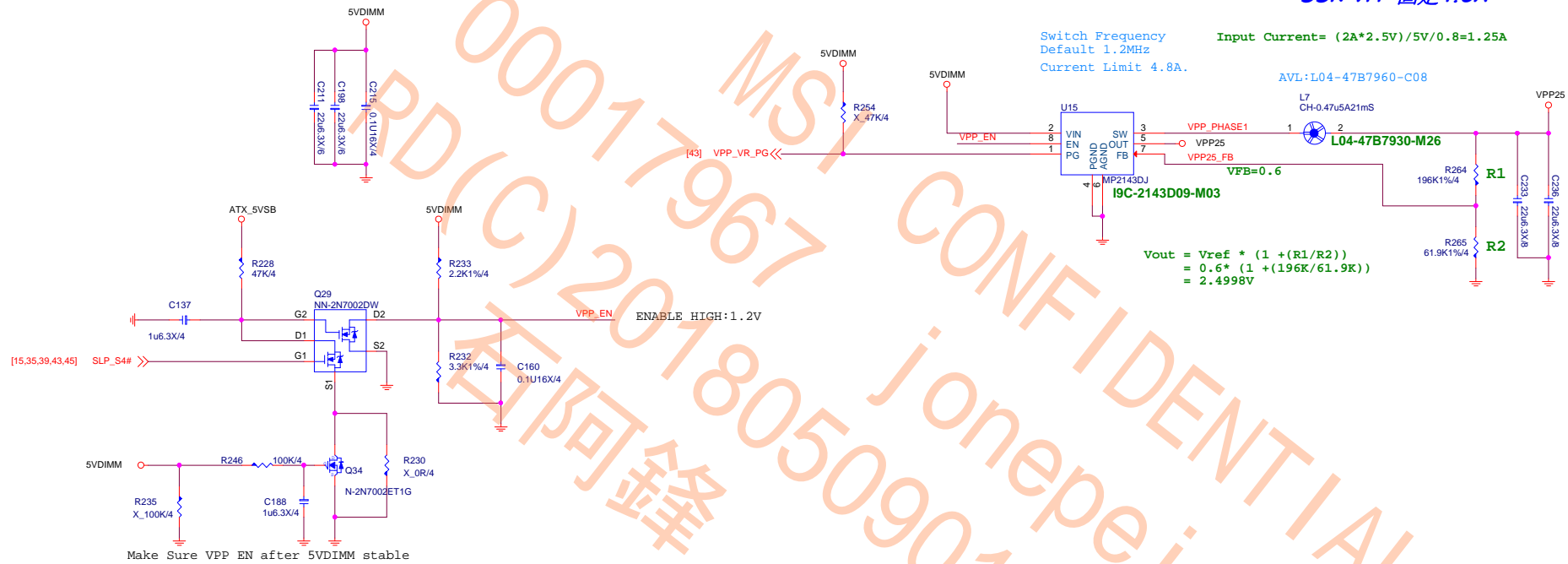
Switch Frequency  
Default 1.2MHz  
Current Limit 4.8A.

Input Current=  $(2A \cdot 2.5V) / 5V / 0.8 = 1.25A$

AVL:L04-47B7960-C08

L7  
CH-0.47u5A21mS

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.6 * (1 + (196K/61.9K)) \\ &= 2.4998V \end{aligned}$$



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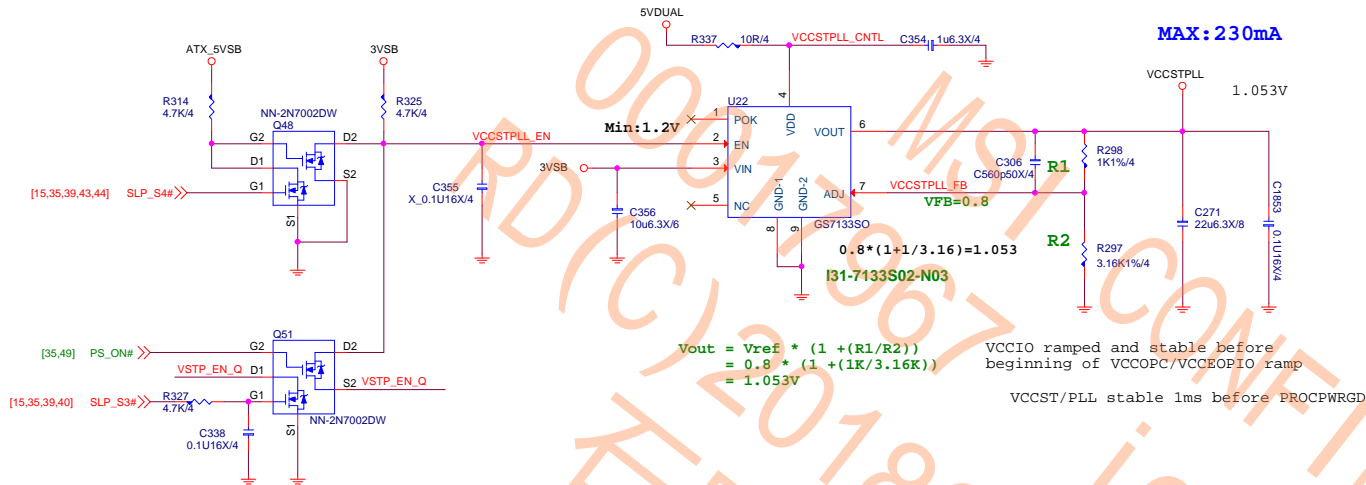
Size Custom	Document Description <b>DDR-MP2143-VPP25</b>
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VCCSTPLL@1.05V/230mA



1P8\_VSB@1.8V/500mA

2017/1/3 Layout空間不足

# PCH\_1VSB@1.05V/11.981A

D03-632BA0C-N03  
Current limit=  $5.6k \cdot 10uA / 4mohm = 14.75A$

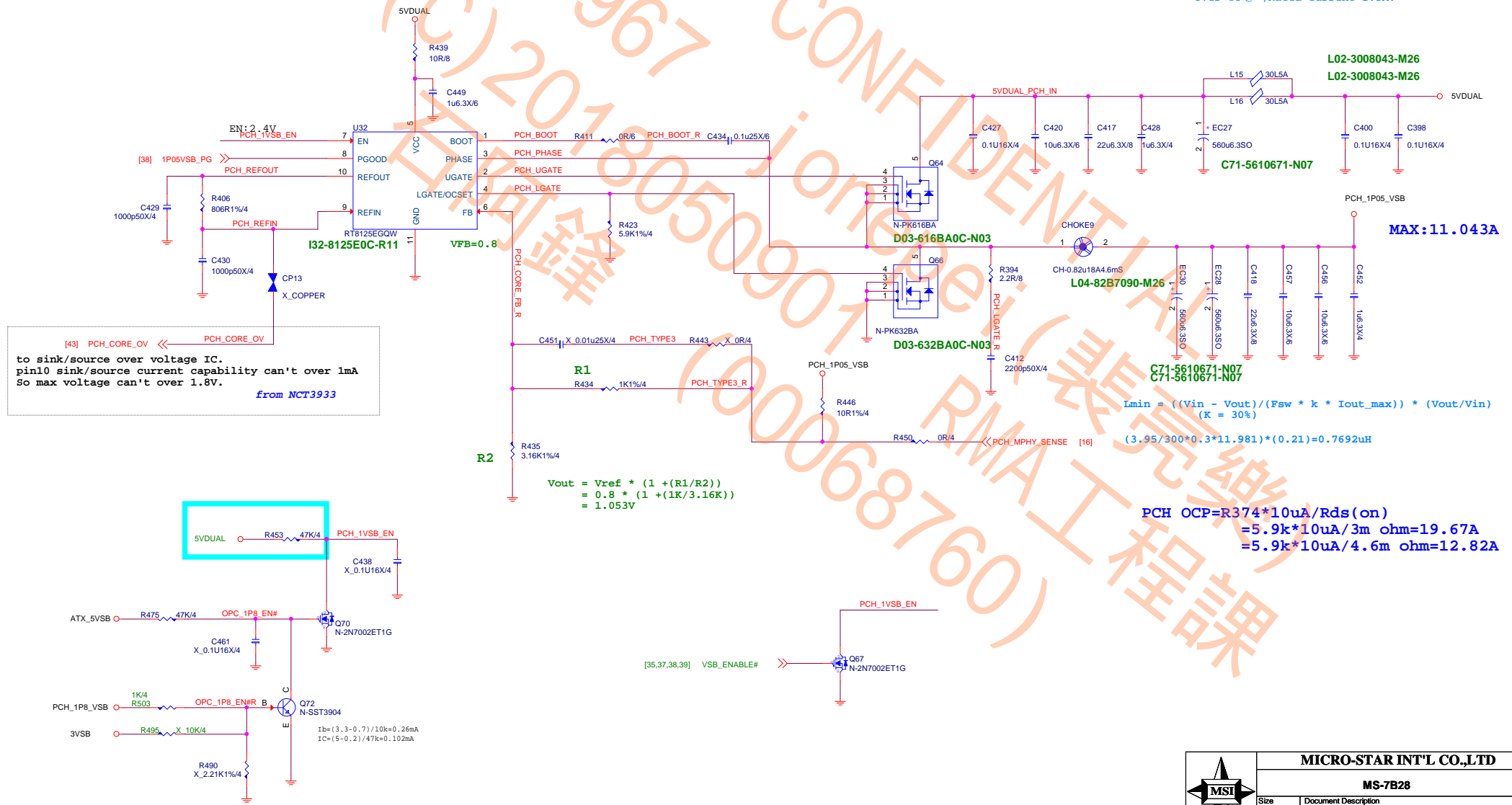
$$I_{rms} = I_{out} \cdot \sqrt{((V_{out}/V_{in}) \cdot (1 - (V_{out}/V_{in})))}$$

$$= 11.981 \cdot 0.407$$

$$= 4.876A$$

$$I_{in} = 11.043A \cdot 1.05V / 0.8 / 5V = 2.898A$$

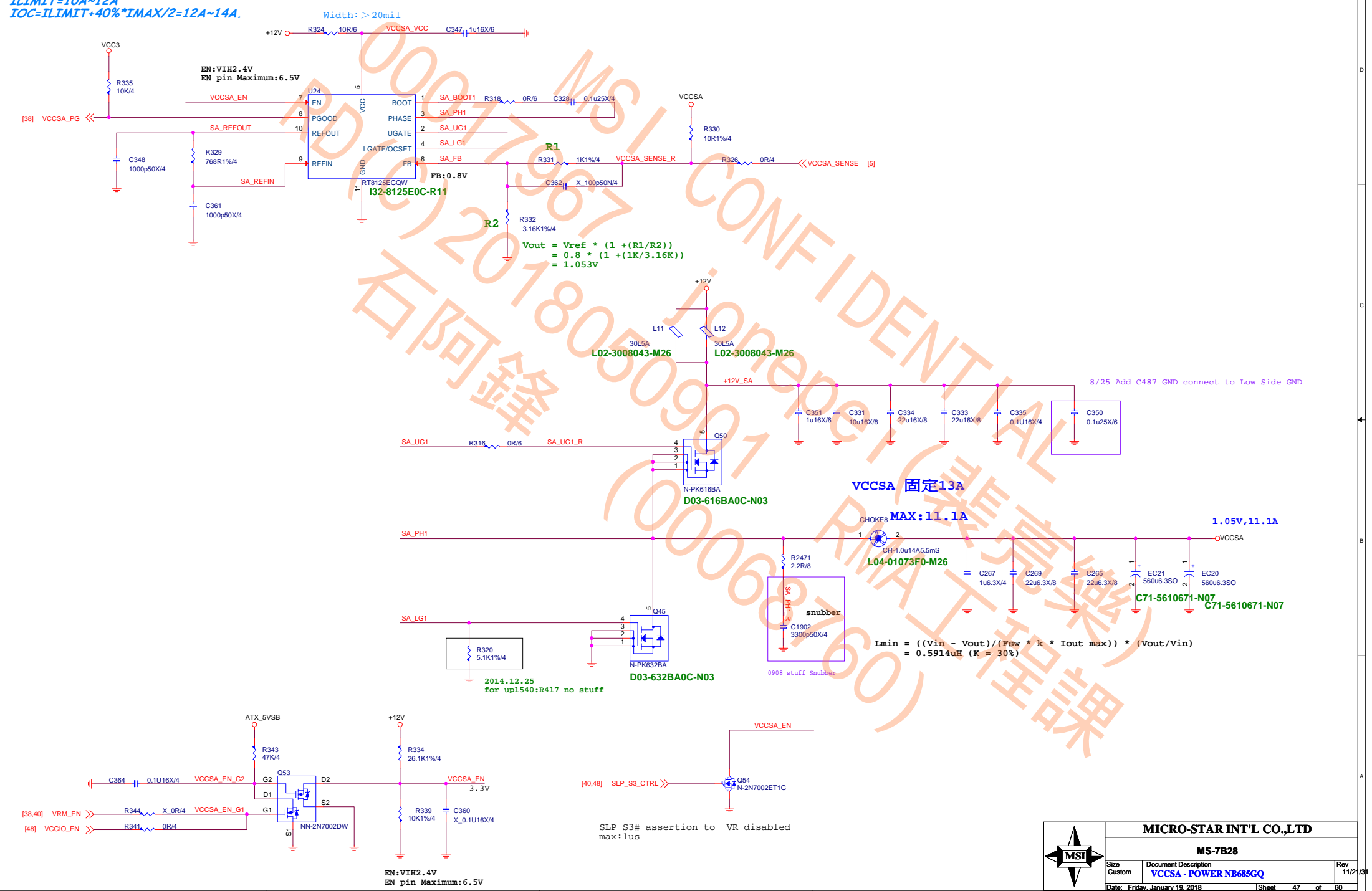
Over 85°C , Rated Current 1.5A.





VCCSA@1.05V/11.1A

IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

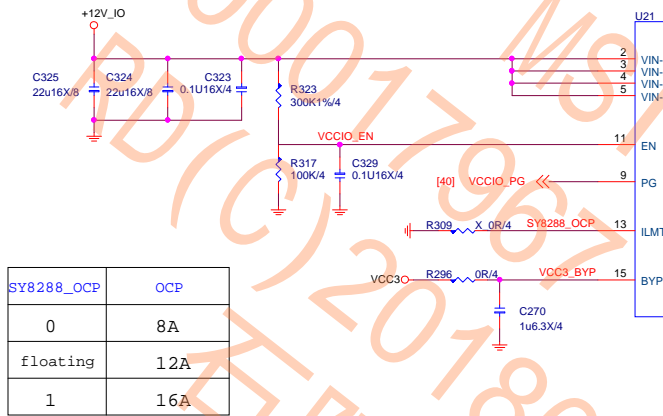
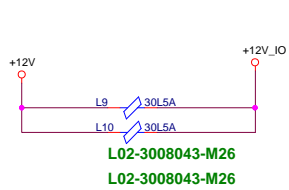


VCCIO@0.95V/6.4A

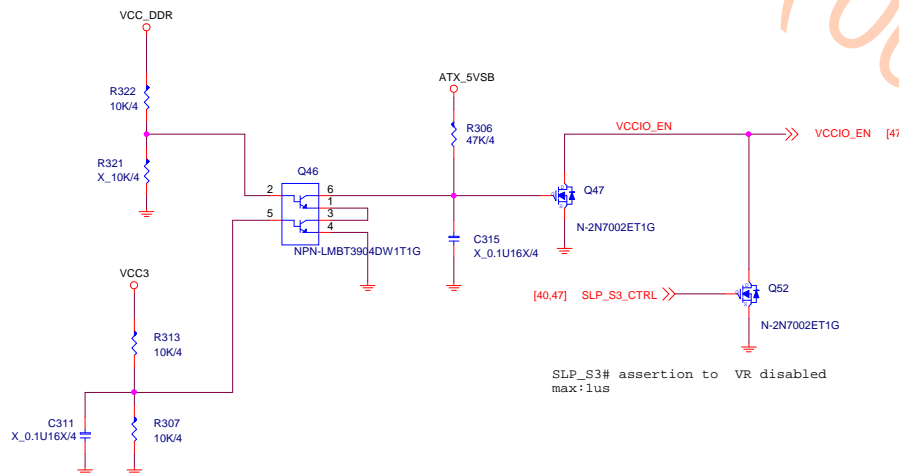
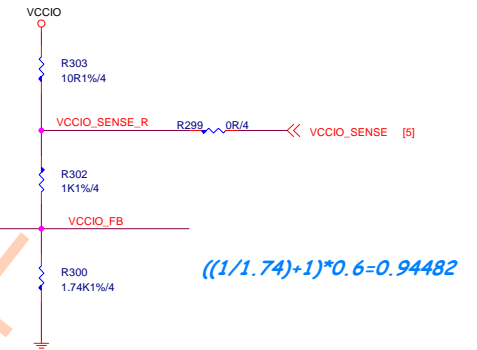
IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

VCCIO 固定12A(floating)

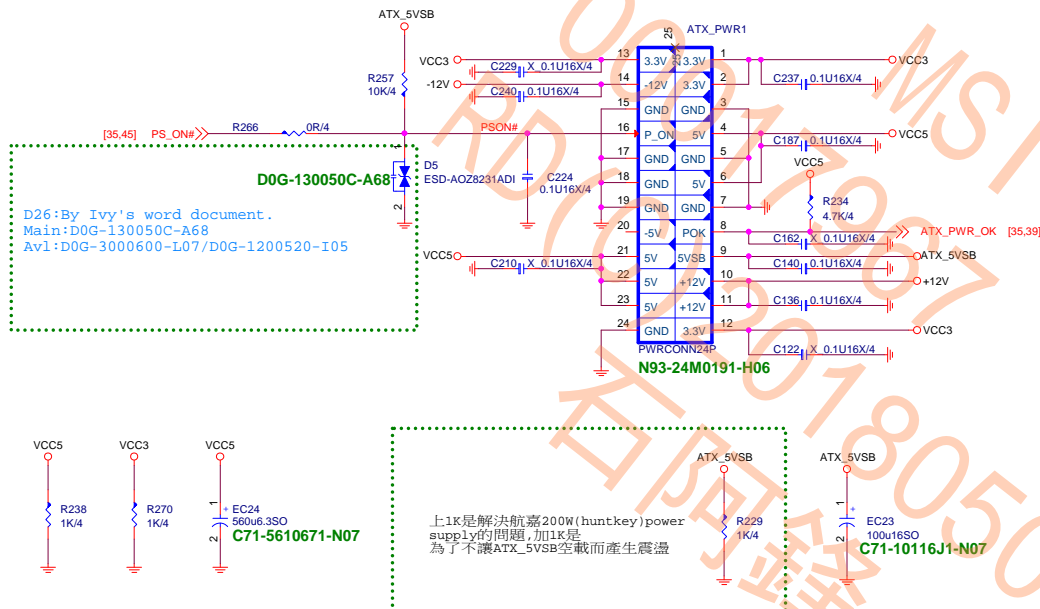
MAX:6.4A



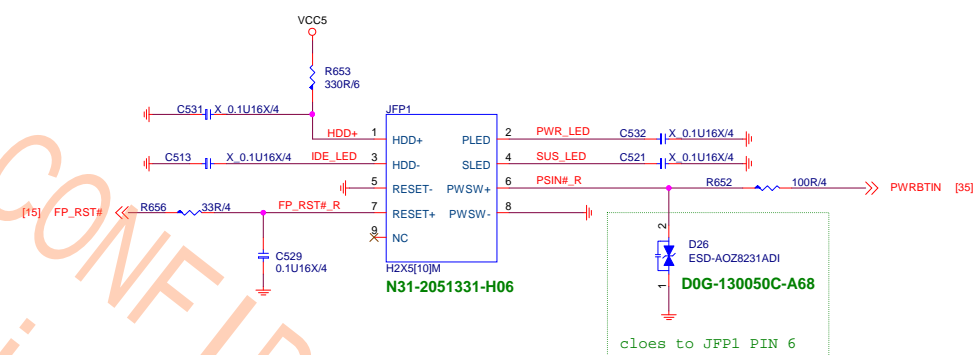
[5] CPU\_CNL\_N >>> CPU\_CNL\_N R301 X 5.9K1%/4  
CPU\_CNL\_N come from CPU PROC\_SELECT#



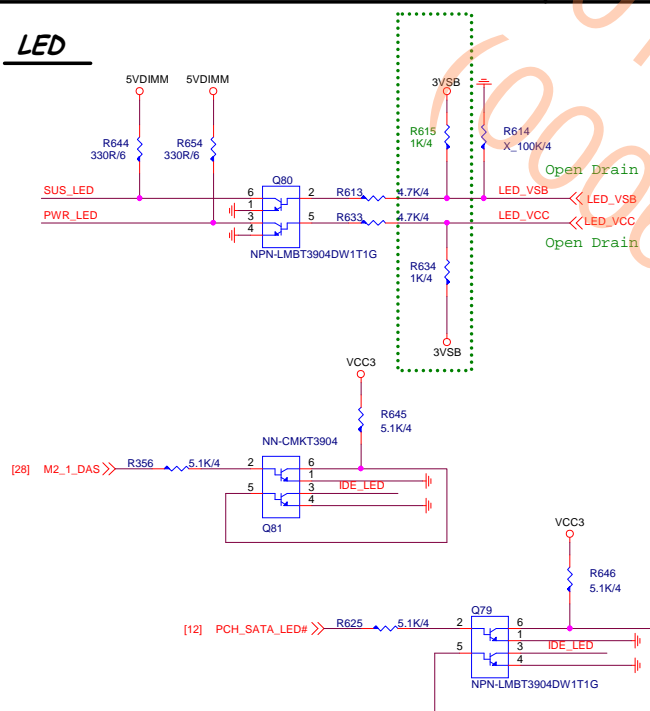
## ATX POWER CONNECTOR



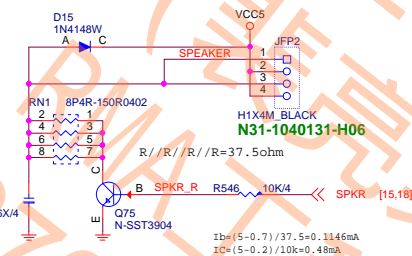
FRONT PANNEL



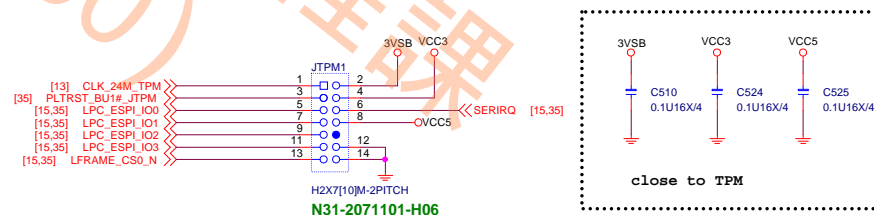
**LED**



### Speaker Pin Header



## TPM



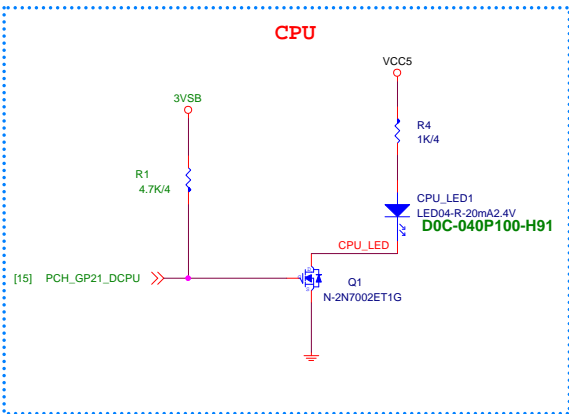
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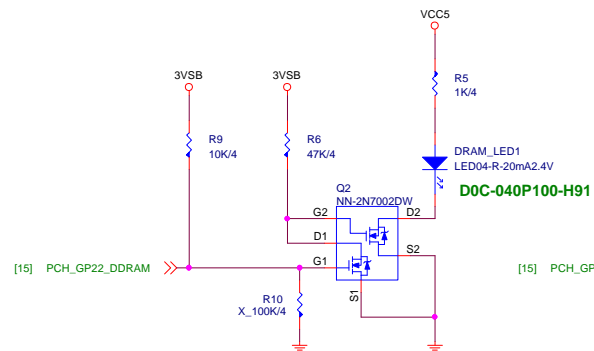
Size Custom	Document Description <b>ATX F_Panel/TPM/MSI_LED</b>	Rev 11/2/3
Date: Friday, January 19, 2018		Sheet 49 of 60

## EZ DEBUG LED

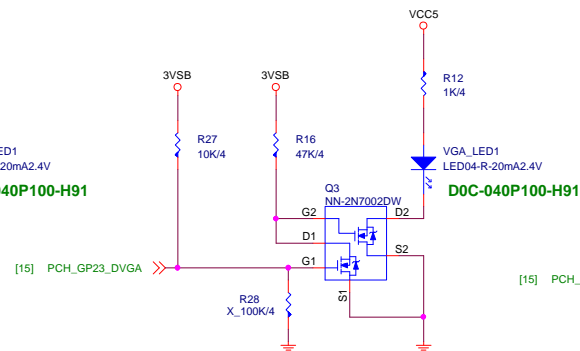
### CPU



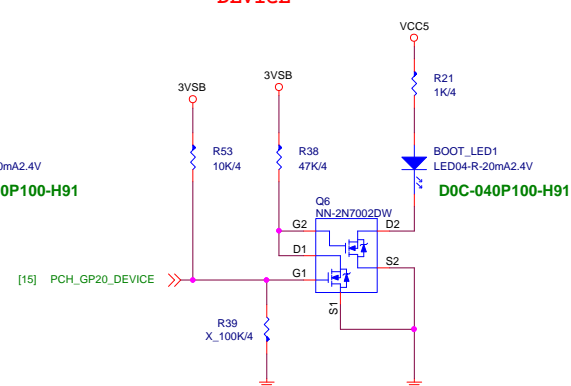
### DRAM



### VGA



### DEVICE



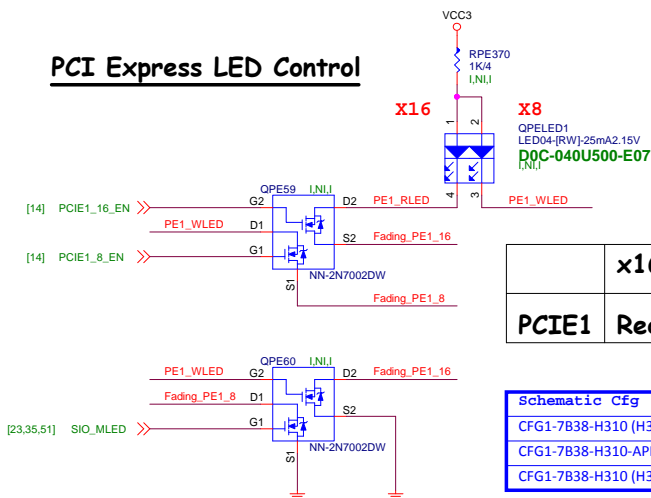
LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

### LED

RED:D0C-040P100-H91  
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91  
AVL:D0C-040S200-E07

## PCI Express LED Control



	x16	x8
PCIE1	Red	White

Schematic Cfg	Project	
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V	C

關機斷電狀態下，3個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。

(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

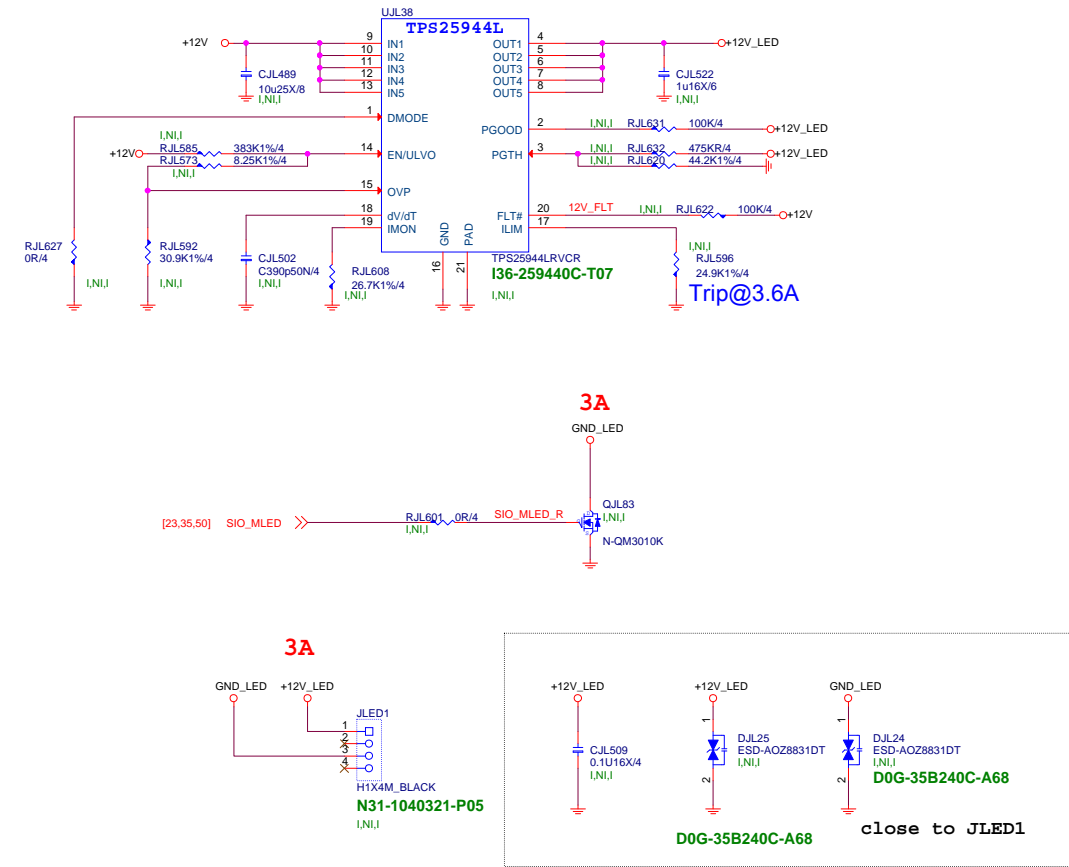


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Size	Document Description	Rev
Custom	ALL LED Control	11/2
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LED Control by SIO(JLED1)



Schematic Cfg	Project	
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	V	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	X	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	V	C

OPTION BOM PARTS

Schematic Cfg	Project
CFG1-7B38-H310 (H310M GAMING PLUS) ver.1.0	A
CFG1-7B38-H310-APRO (H310-A Pro) ver.2.0	B
CFG1-7B38-H310 (H310-A GAMING ARCTIC) ver.3.0	C

5010 Level

O EZ GP

MS10/50C 1630

LED04-R-20mA2.4V\_1608-HF

D0C-040P100-H91

Red

PD0-07B2810-E48

PD0-07B2811-G37

O PCB GP

7B28\_11

O EZ PRO

MS10/50C 1630

LED04-R-20mA2.4V\_1608-HF

D0C-040T200-H91

White

PK0-07B2820-E48

PK0-07B2821-G37

O PCB PRO

7B28\_21

O EZ GAR

MS10/50C 1630

LED04-R-20mA2.4V\_1608-HF

D0C-040T200-H91

White




PS0-07B2830-E48

PS0-07B2831-G37

O PCB GAR

7B28\_31

PCB



5020 Level

O AUDLED GP

AUD10-1630

LED04-BR125mA2.35V

D0C-040S600-E07

Red

O AUDLED PRO


AUD10-1630

LED04-W-20mA3.9V\_1608-RH

D0C-040T300-H91

White

AUDIO LED



60 Level

O REARU3 GP


LANC-03

USBAX2M\_RED-RH-2

USB\_C1\_24\_2

N53-18M0201-L06

REAR U3




O REARU3 PRO

LANC-03

USBAX2M\_BLUE-RH-6

USB\_C1\_24\_2

N53-18M0091-F02




O REARU3 GAR

LANC-03

USBAX2M\_RED-RH-2

USB\_C1\_24\_2

N53-18M0201-L06



O DDRSL0T GP

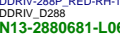
DDR-160C

DDRIV-288P\_RED-RH-1

DDRIV\_D288

N13-2880681-L06

DDR Slot



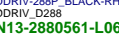
O DDRSL0T PRO

DDR-160C

DDRIV-288P\_BLACK-RH-21

DDRIV\_D288

N13-2880561-L06




O DDRSL0T GAR

DDR-160C

DDRIV-288P\_BLACK-RH-21

DDRIV\_D288

N13-2880521-L06




O PCIE16 GP

PCI6-16

SLOT-PCI164P\_RED-2PITCH-RH-1

N11-1641671-L06

PCIEx16 Slot




O PCIE16 PRO

PCI6-16

SLOT-PCI164P\_BLACK-2PITCH-RH-38

N11-1641221-L06




O PCIE16 GAR

PCI6-16

SLOT-PCI164P\_WHITE-2PITCH-RH-4

N11-1641601-L06



O VGA GP

VGA

DVI24P\_BLACK-RH-17

N5B-24F0771-EB6

DVI



O VGA GAR

VGA

DVI24P\_BLACK-RH-17

N5B-24F0771-EB6



O VGA+DVI PRO

VGA+DVI

VGA\_DVI-RH-31

N58-39F0371-EB6

VGA+DVI



O LA GP

B310

Lable

MKT

G51-M1SPM62-Q13

PACK LABEL



O LA PRO

B310

Lable

MKT

G51-M1SPM61-Q13



O LA GAR

B310

Lable

MKT

G51-M1SPM60-Q13



O PHSK GP

HS0409490

HS-0409490

E31-0409490-K08

PCH Heatsink



O PHSK PRO

HS0409430

HS-0409430

E31-0409430-K08



O PHSK GAR

HS0409520

HS-0409520

E31-0409520-K08



O CHSK GP

CPU

鐵座

CPU\_H1

E21-7869020-F02

CPU Heatsink



O CHSK PRO

CPU

鐵座

CPU\_H1

E21-7869020-F02



O CHSK GAR

CPU

鐵座

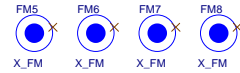
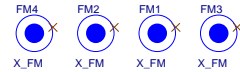
CPU\_H1

E21-7A45010-L06

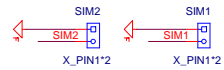




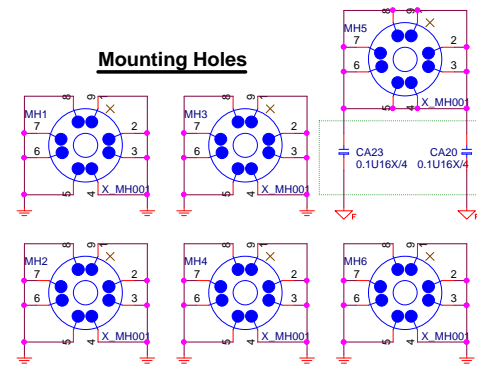
## Optical Fiducial Marks-120



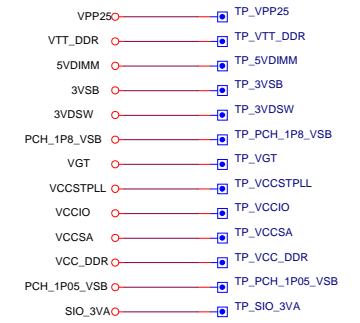
## Simulation



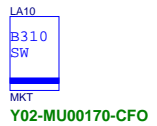
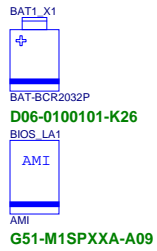
## Mounting Holes



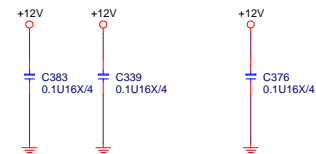
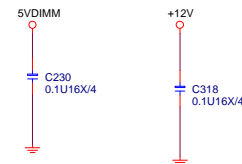
HOLES\_4S



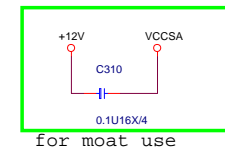
## Near SIO CHIP



## return path



For M2 reference +12V USE  
please close to under M2



for moat use